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DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1851B

I²C BUS-COMPATIBLE US MTS PROCESSING LSI

The μPC1851B is an integrated circuit for US MTS (Multiplexed Television Sound) system with the addition of the I²C bus interface. All functions required for US MTS system are incorporated on a single chip.

The μPC1851B allows users to switch modes, control volume and tone, and adjust the separation circuit through the I²C bus.

FEATURES

- Stereo demodulation, SAP (Sub Audio Program) demodulation, dbx noise reduction decoding, I²C bus interface, input selector (2 channels), surround processor (1 phase), volume and tone control circuits incorporated on a single chip
- Mode switching, volume and tone control, and separation adjustment through the I²C bus
- Power supply: 8 V to 10 V
- On-chip input attenuator for simple interface with intermediate frequency processing IC (I²C bus control)
- Output level: 1.4 V_{p-p} (with L+R signals, 100 % modulation)

APPLICATION

- TV sets and VCRs for north America

ORDERING INFORMATION

Part Number	Package
μPC1851BCU	42-pin plastic SDIP (15.24 mm (600))

The μPC1851B is available only to licensees of THAT Corporation.
For information, please call: (508) 229-2500 (U.S.A), or (03) 5790-5391 (Tokyo).

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Printed in Japan

The mark ★ shows major revised points.

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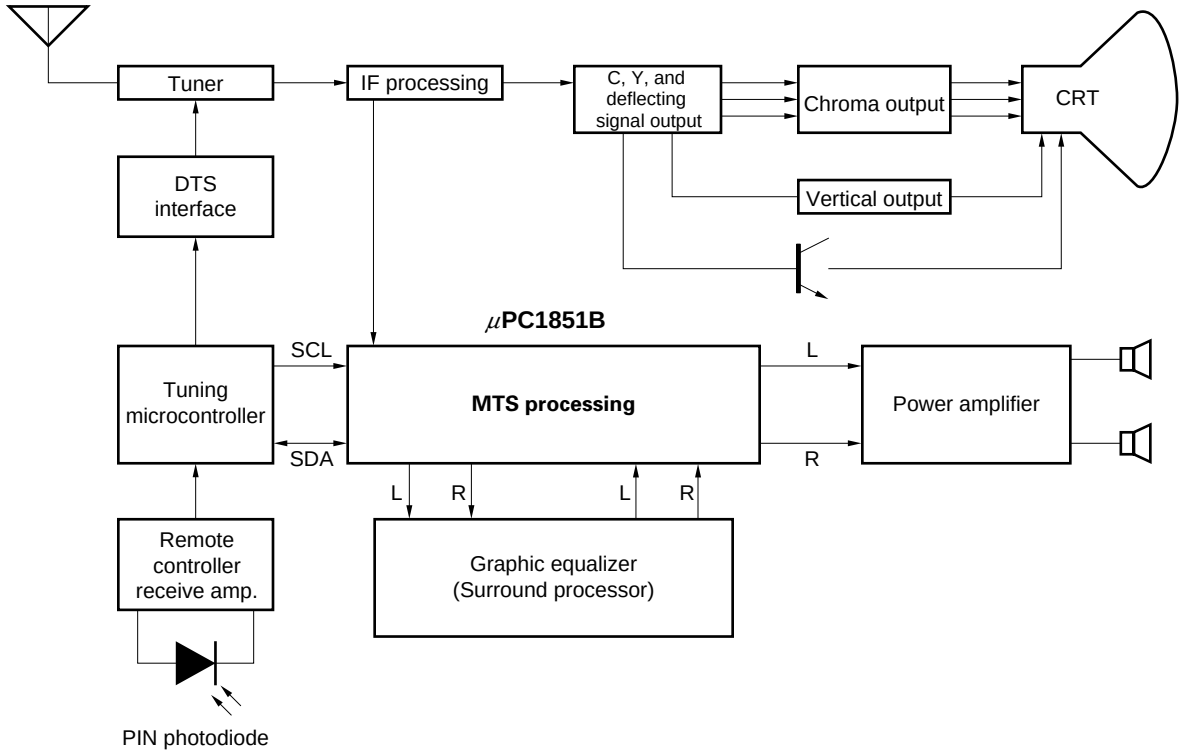
SYSTEM BLOCK DIAGRAM

● **TV**



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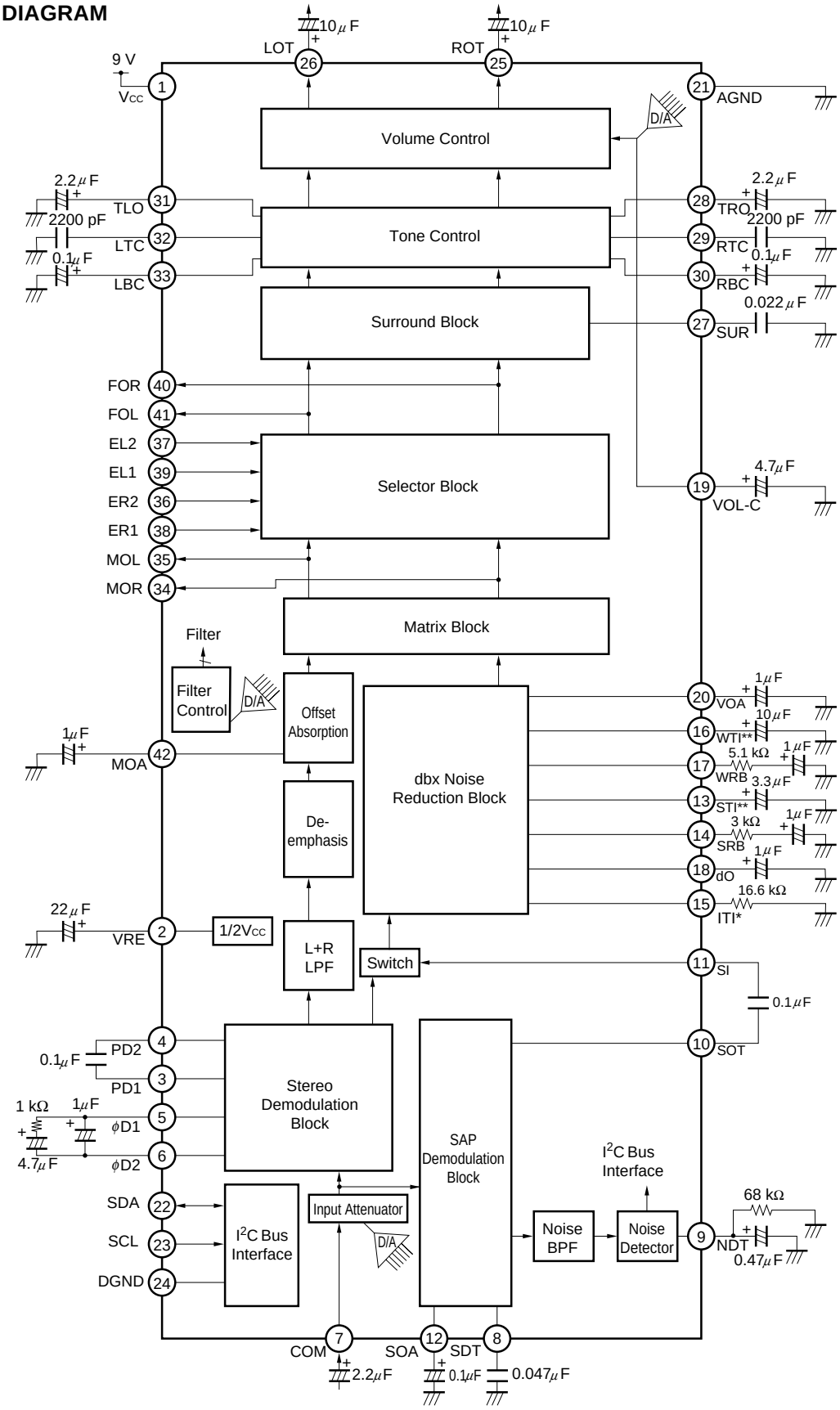
BLOCK DIAGRAM



Remark Use the followings for external parts.
Resistor (*): Metal film resistor (± 1 %). Unless otherwise specified; ±5 %
Capacitors (**): Tantalum capacitor (±10 %). Unless otherwise specified; ±20 %

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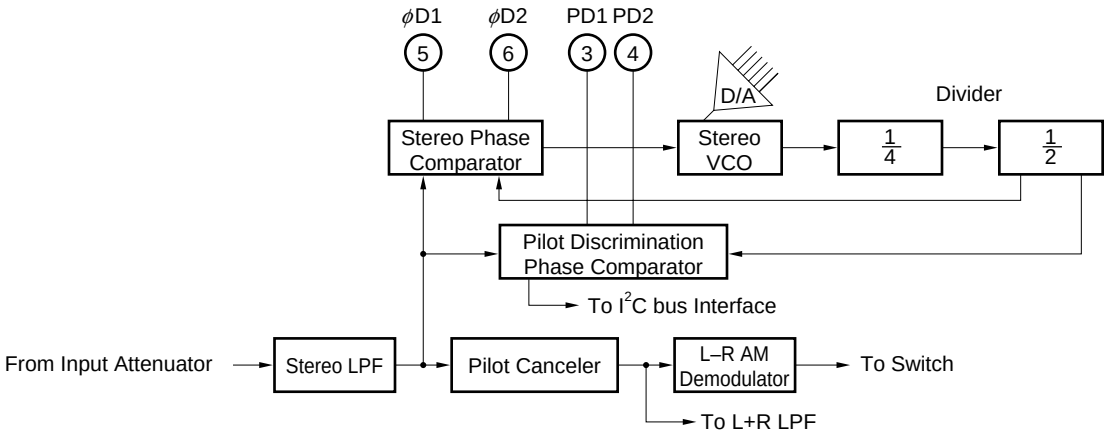
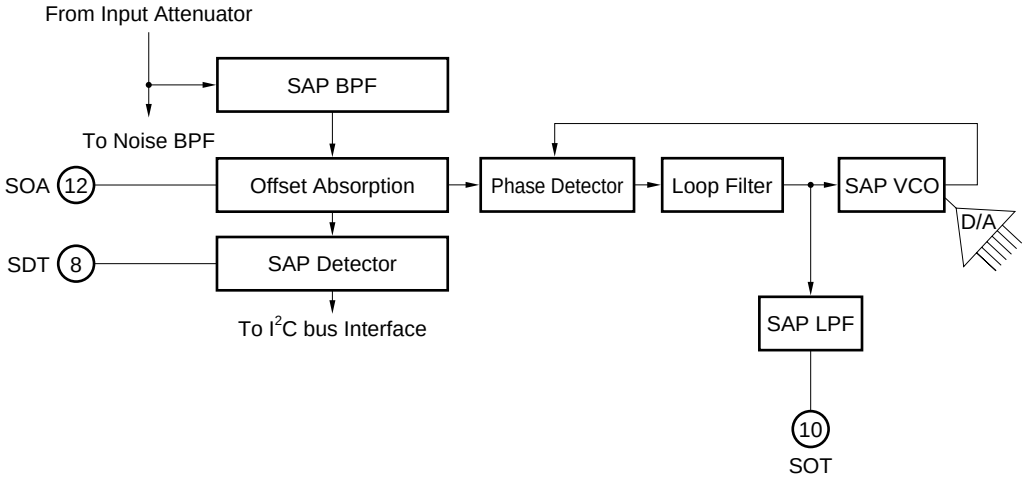
STEREO DEMODULATION BLOCK



SAP DEMODULATION BLOCK



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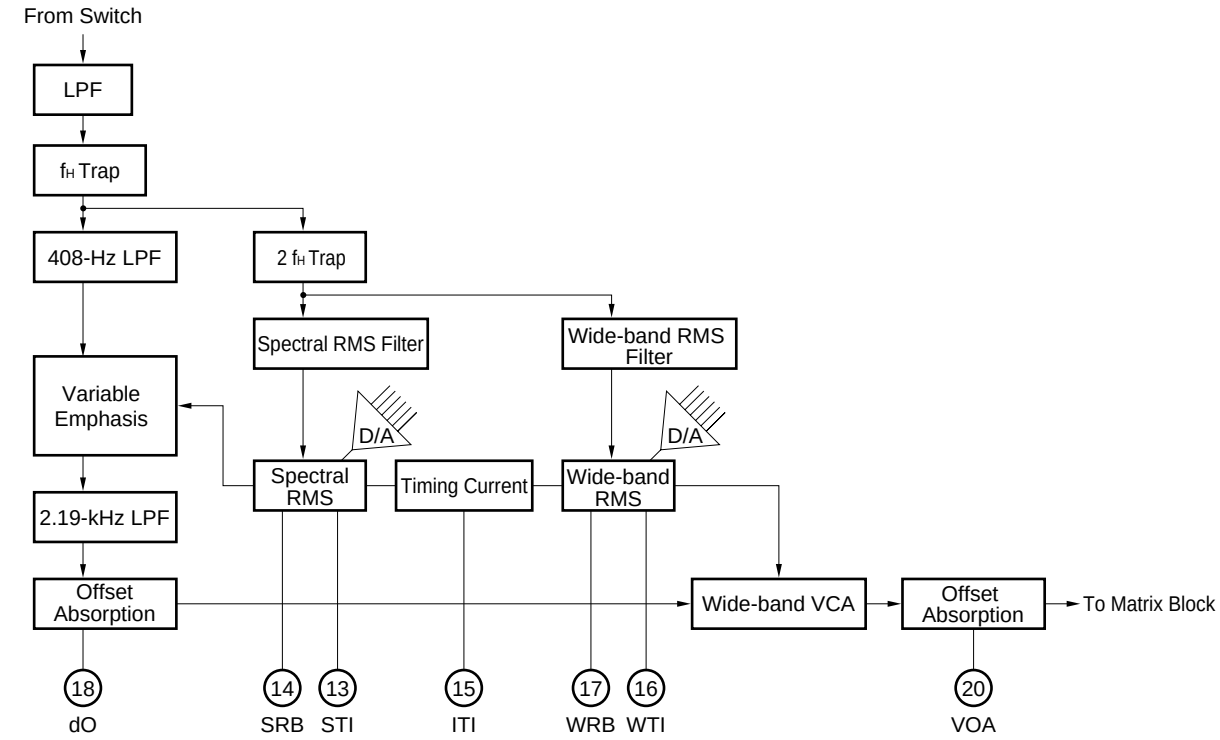
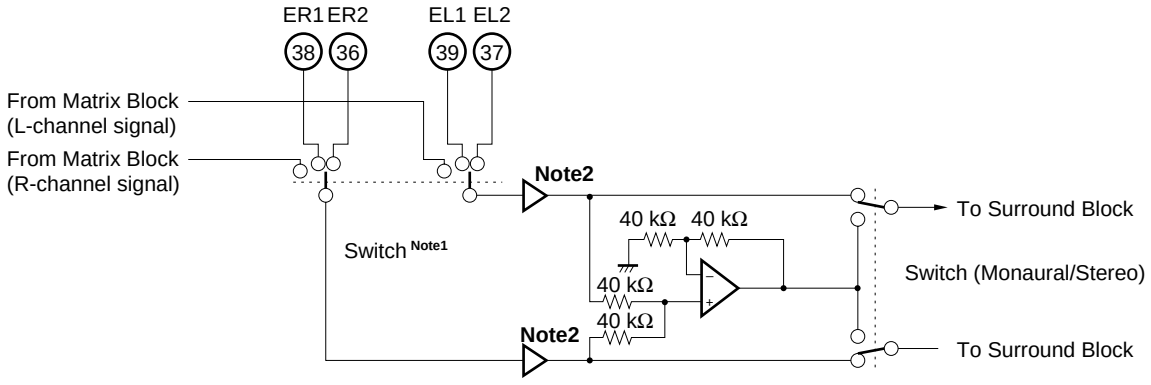
dbx NOISE REDUCTION BLOCK



SELECTOR BLOCK



Notes 1. Switch (TV signal/External input 1/External input 2).

2. The input gain 0 dB/6 dB can be selected by the command of the I²C bus (refer to **4.3 (5) Input gain**).

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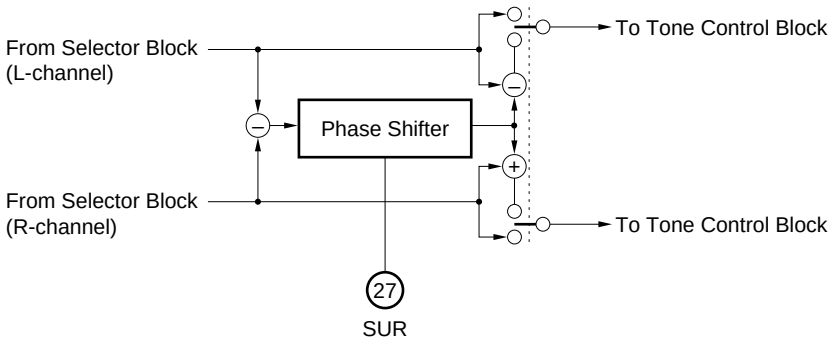
SURROUND BLOCK



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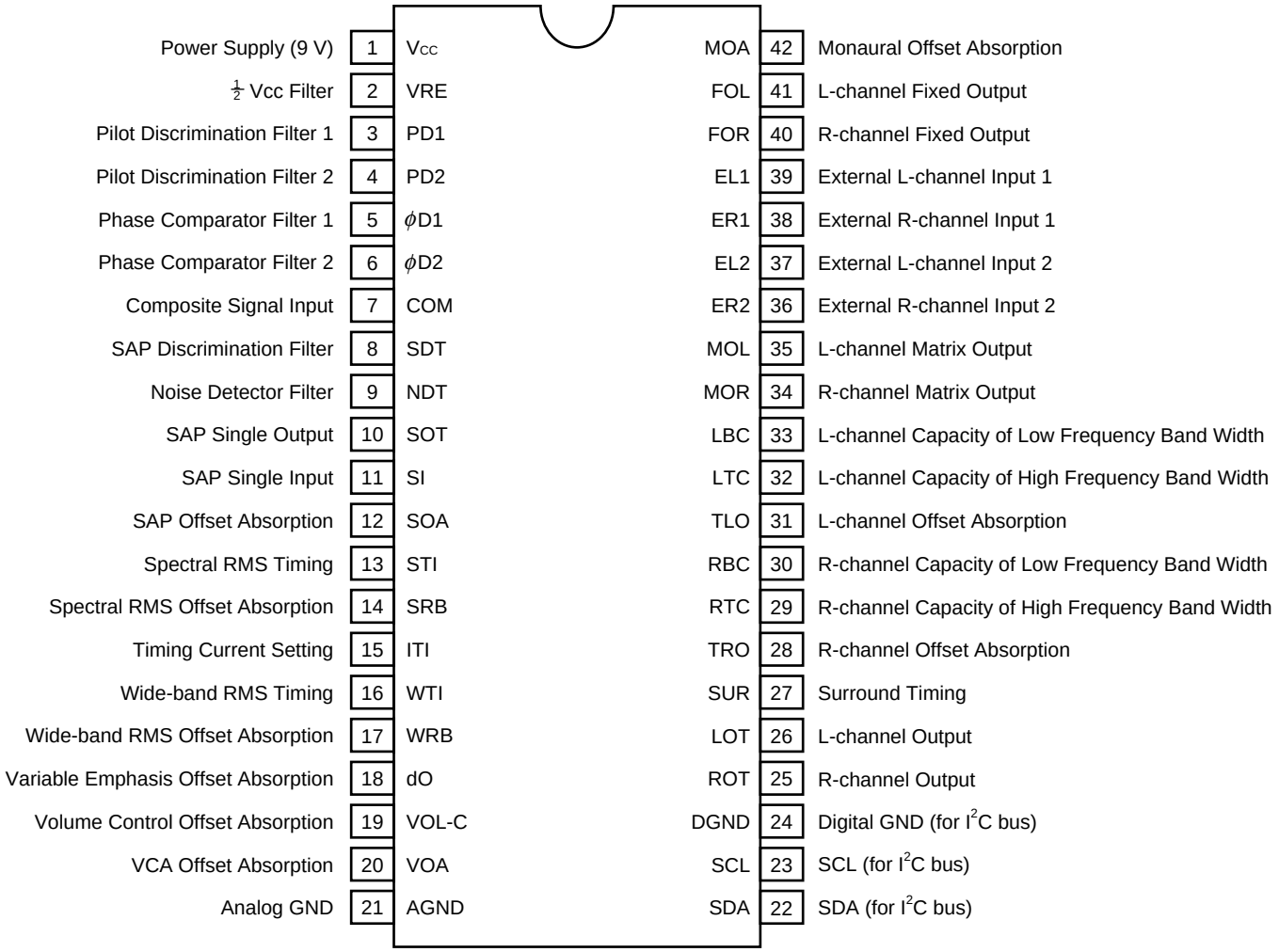
PIN CONFIGURATION (Top View)

42-pin plastic SDIP (15.24 mm (600))

- μPC1851BCU



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CONTENTS

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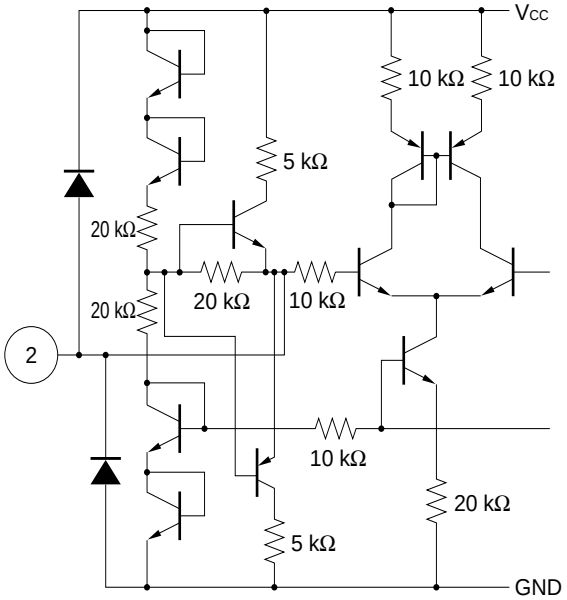
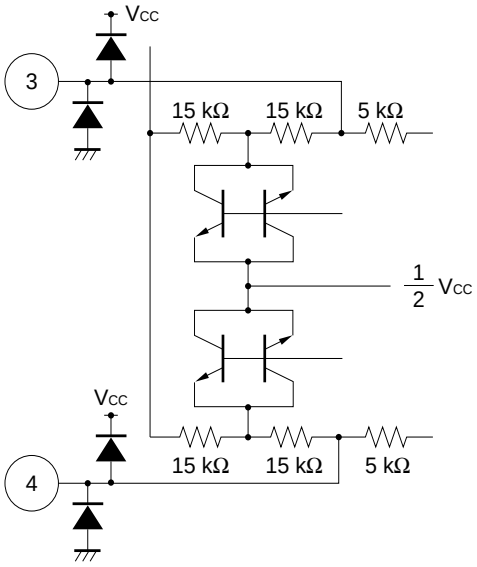
1. PIN EQUIVALENT CIRCUITS

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
1	Power Supply (9 V)	V_{CC}	
2	$\frac{1}{2}V_{CC}$ Filter	VRE	
3	Pilot Discrimination Filter 1	PD1	
4	Pilot Discrimination Filter 2	PD2	

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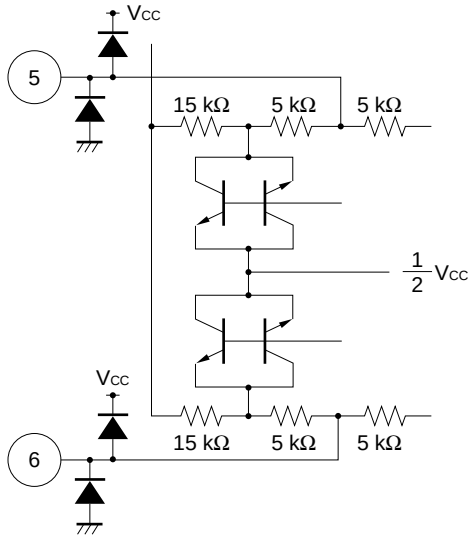
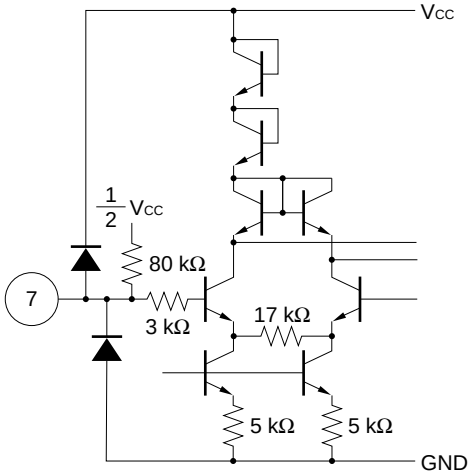
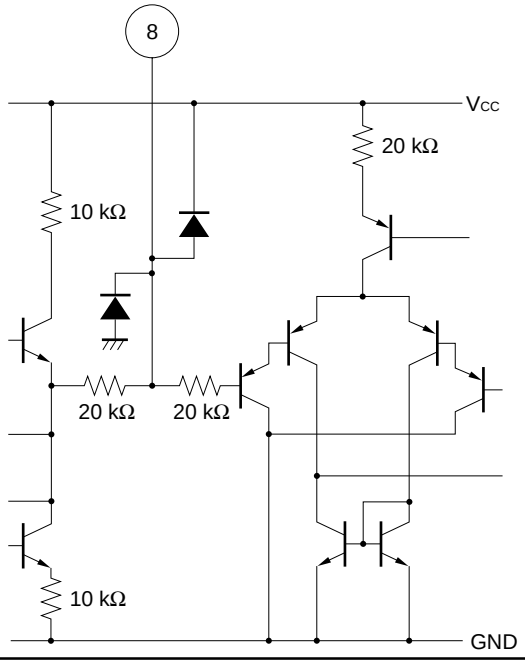
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
5	Phase Comparator Filter 1	φD1	
6	Phase Comparator Filter 2	φD2	
7	Composite Signal Input	COM	
8	SAP Discrimination Filter	SDT	

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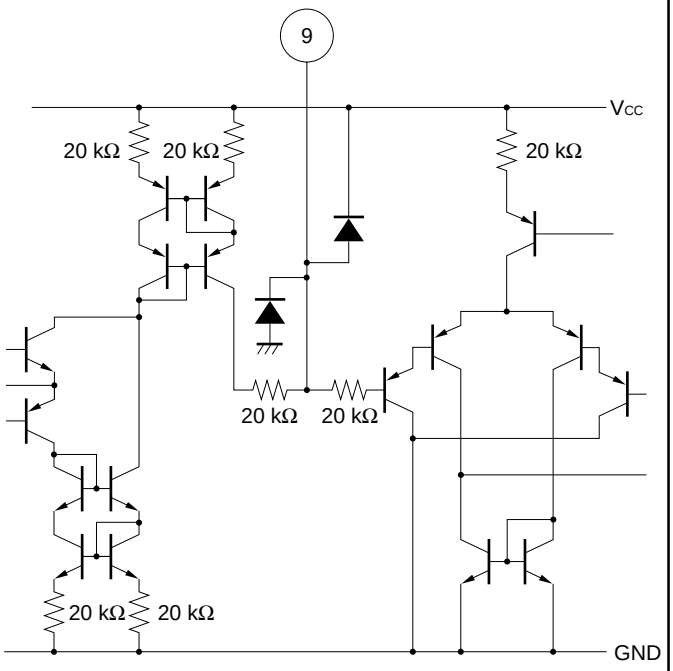
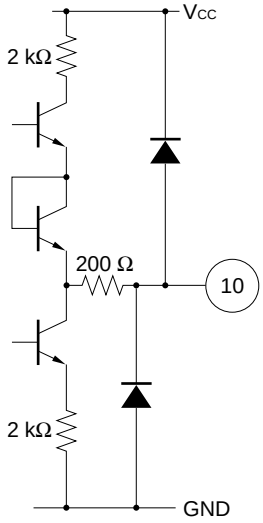
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
9	Noise Detector Filter	NDT	
10	SAP Single Output	SOT	

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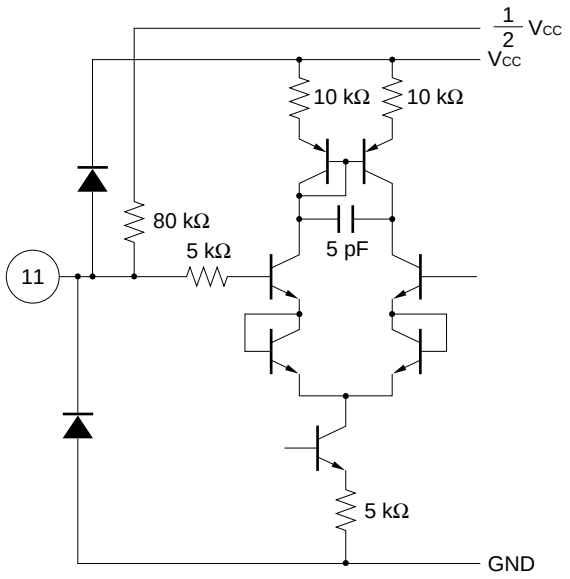
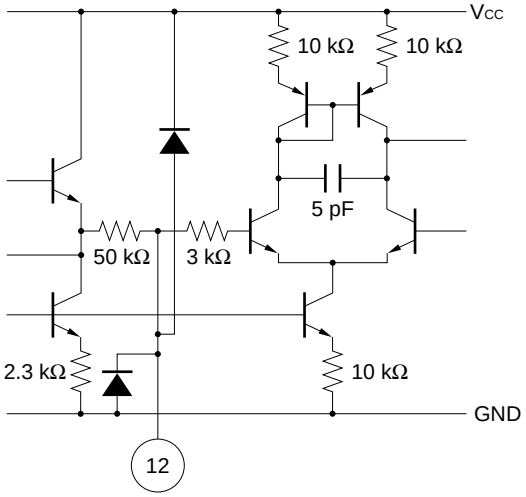
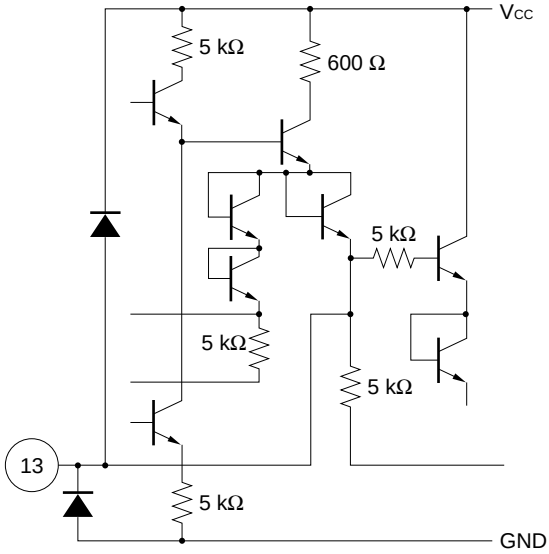
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
11	SAP Single Input	SI	
12	SAP Offset Absorption	SOA	
13	Spectral RMS Timing	STI	

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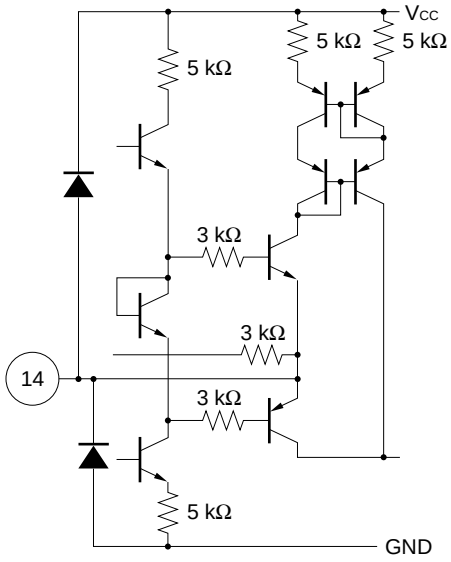
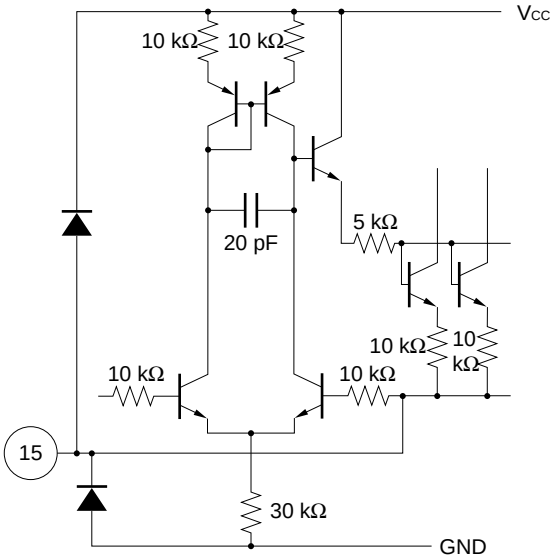
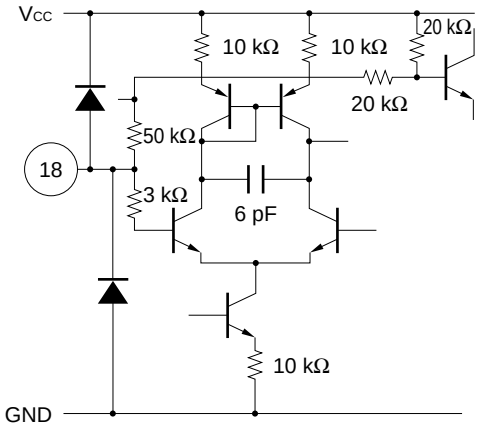
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
14	Spectral RMS Offset Absorption	SRB	
15	Timing Current Setting	ITI	
16	Wide-band RMS Timing	WTI	Same as pin 13
17	Wide-band RMS Offset Absorption	WRB	Same as pin 14
18	Variable Emphasis Offset Absorption	dO	

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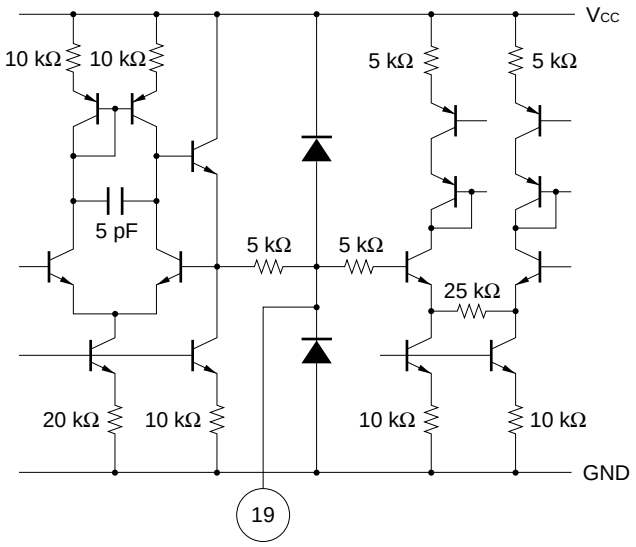
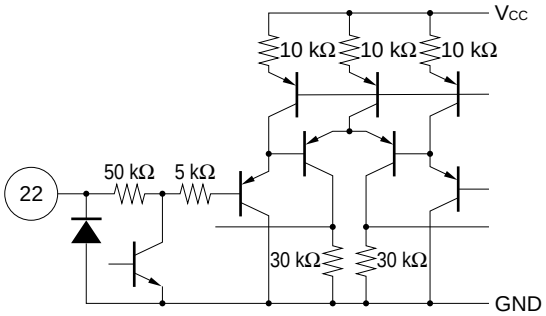
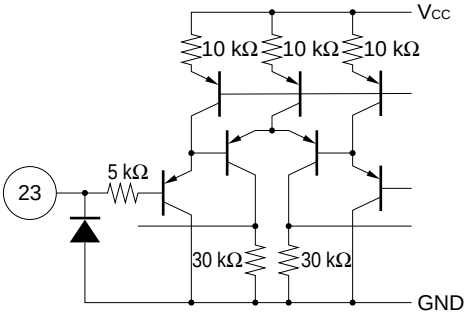
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
19	Volume Control Offset Absorption	VOL-C	
20	VCA Offset Absorption	VOA	Same as pin 12
21	Analog GND	AGND	
22	SDA (for I²C bus) **Note**	SDA	
23	SCL (for I²C bus) **Note**	SCL	
24	Digital GND (for I²C bus)	DGND	

Note A protection diode on the V_{CC} side is deleted not so as to pull the voltage of I²C bus line down to 0 V while the power supply is off (V_{CC} = 0 V).

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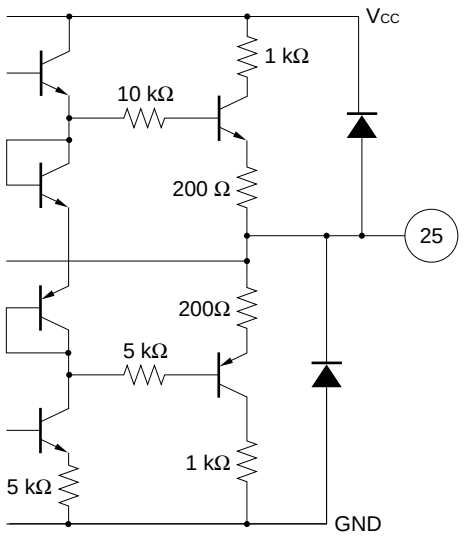
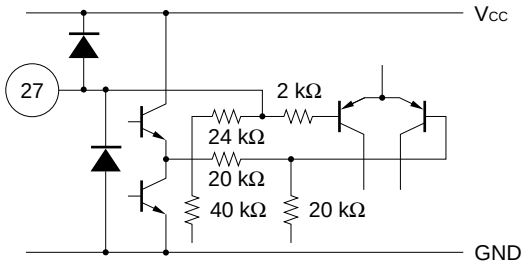
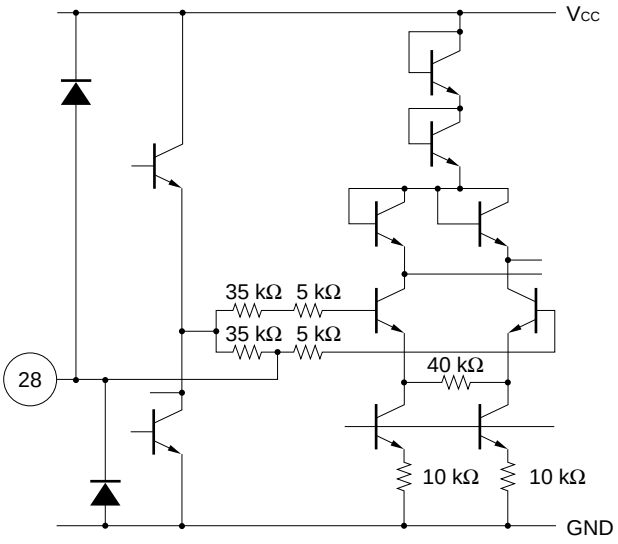
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
25	R-channel Output	ROT	
26	L-channel Output	LOT	Same as pin 25
27	Surround Timing	SUR	
28	R-channel Offset Absorption	TRO	

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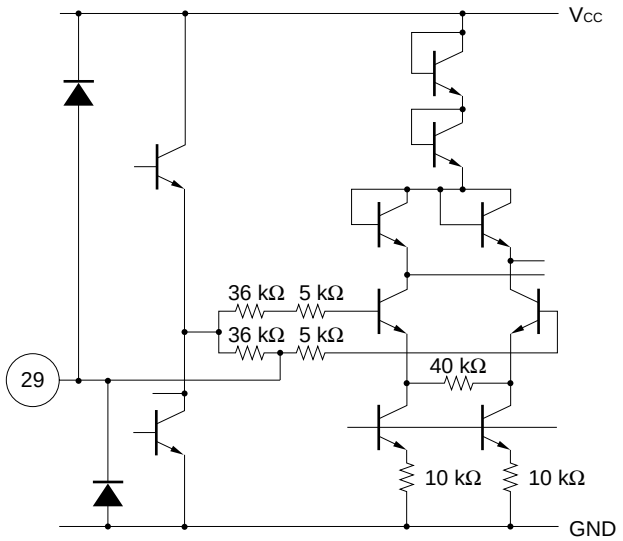
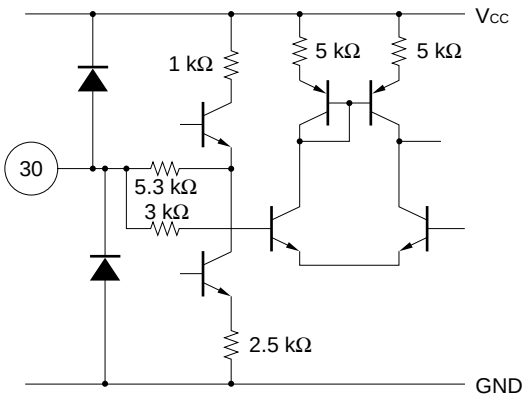
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
29	R-channel Capacity of High Frequency Band Width	RTC	
30	R-channel Capacity of Low Frequency Band Width	RBC	
31	L-channel Offset Absorption	TLO	Same as 28
32	L-channel Capacity of High Frequency Band Width	LTC	Same as 29
33	L-channel Capacity of Low Frequency Band Width	LBC	Same as 30
34	R-channel Matrix Output	MOR	Same as 25
35	L-channel Matrix Output	MOL	

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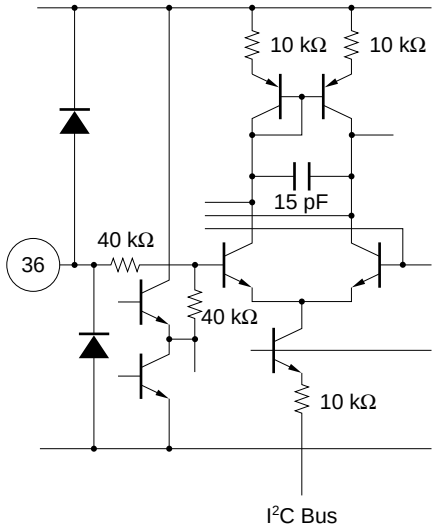
Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
36	External R-channel Input 2	ER2	
37	External L-channel Input 2	EL2	
38	External R-channel Input 1	ER1	
39	External L-channel Input 1	EL1	
40	R-channel Fixed Output	FOR	Same as pin 25
41	L-channel Fixed Output	FOL	
42	Monaural Offset Absorption	MOA	Same as pin 18

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2. BLOCK FUNCTIONS

2.1 Stereo Demodulation Block

(1) Stereo LPF

This filter eliminates signals in the vicinity of 5 f_H to 6 f_H, such as SAP (Sub Audio Program) (5 f_H) and telemetry signals (6.5 f_H) . The μPC1851B's internal L–R demodulator, which uses a double-balanced circuit, demodulates L–R signals by multiplication of the L–R signal with the signal at the L–R carrier frequency (2 f_H). The L–R signal tends to receive interference from the 6 f_H signal because a square waveform is used as the switching carrier in this method. To eliminate this interference, the μPC1851B incorporates traps at 5 f_H and 6 f_H. The filter response is adjusted by setting the FILTER SETTING bits (Write register, subaddress 02H, bits D0 to D5).

(2) Stereo Phase Comparator

The 8 f_H signal generated at the Stereo VCO is divided by 8 (4 × 2) and then multiplied by the pilot signal passed through the stereo LPF. The two signals differ from each other by 90 degrees in terms of phase.

The resistor and capacitor connected to the ϕD1 and ϕD2 pins form a filter that smoothes the phase error signal output from the Stereo Phase Comparator, converting the error signal to the DC voltage. When the voltage difference between ϕD1 and ϕD2 pins becomes 0 V (strictly speaking, not 0 V by the internal offset voltage), the VCO runs at 8 f_H.

The lag/lead filter externally connected to the pins ϕD1 and ϕD2 determines the capture range.

(3) Stereo VCO

The Stereo VCO runs at 8 f_H with the internal capacitor. The frequency is adjusted by setting the STEREO VCO SETTING bits (Write register, subaddress 01H, bits D0 to D5).

(4) Divider (Flip-flop)

Produces two separate f_H signals: the inphase f_H signal, and the f_H signal differing by 90 degrees from the input pilot signal by dividing the 8 f_H frequency from the Stereo VCO by 8 (4 × 2).

(5) Pilot Discrimination Phase Comparator (Level detector)

Multiplies the pilot signal from the COM pin with the inphase f_H signal from the divider. The resulting signal is smoothed by passing it through the external filter connected to the PD1 and PD2 pins and converted into DC voltage that is used to determine whether or not a stereo pilot is present (Read register, bit D6).

(6) Pilot Canceler

The f_H signal from the divider is added to the stereo signal matrix depending on the level of the input pilot signal to cancel the pilot signal.

(7) L+R LPF

This LPF which has traps at f_H and 24 kHz, allows only the monaural signal to pass through. The filter response is adjusted by setting the FILTER SETTING bit (Write register, subaddress 02H, bits D0 to D5).

(8) De-emphasis

The 75-μs de-emphasis filter is for the monaural signal. The response is adjusted by setting the FILTER SETTING bit (Write register, subaddress 02H, bits D0 to D5).

(9) L–R AM Demodulator

Demodulates the L–R AM-DSB modulated signal by multiplying with the 2-f_H signal which is synchronized to the pilot signal. The 2-f_H square wave is used as the switching carrier.

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2.2 SAP Demodulation Block

(1) SAP BPF

Picks up the SAP signal by the 50-kHz and 102-kHz traps and a response peak at 5 f_H. The filter response is adjusted by setting the FILTER SETTING bit (Write register, subaddress 02H, bits D0 to D5).

(2) Noise BPF

The μPC1851B monitors signals picked up by the noise BPF (f_O ≒ 180 kHz), and distinguishes noise from signals. By this method, the μPC1851B prevents faulty SAP detection in a weak electric field. The filter response is adjusted by setting the FILTER SETTING bit (Write register, subaddress 02H, bits D0 to D5).

(3) Noise Detector

Performs full-wave rectification of noise from noise BPF, changes it to the DC voltage, and inputs it to the comparator. When the noise level exceeds the reference level, the Noise detection bit (Read register, bit D4) turns "1".

The sensitivity and time constant of the circuit are adjusted by setting the values of the resistor and capacitor connected to the NDT pin.

(4) SAP Detector

Detects the signal from the SAP BPF and smoothes it through the SDT pin and inputs it to the comparator. When it detects the SAP signal, the SAP broadcast (Broadcast status) (Read register, bit D5) turns "1".

(5) SAP Demodulator

The SAP demodulator consists of a phase detector, a loop filter and an SAP VCO (PLL detection circuit).

The SAP VCO oscillates at 10 f_H, and performs phase comparison between the signal divided by 2 of the SAP VCO frequency and the SAP signal to make the PLL. The SAP VCO oscillating frequency is adjusted by setting the SAP VCO SETTING bit (Write register, subaddress 05H, bits D0 to D5).

(6) SAP LPF

Eliminates the SAP carrier and high-frequency buzz. The filter consists of a 2nd-order LPF and f_H trap filter. The filter response is adjusted by setting the FILTER SETTING bit (Write register, subaddress 02H, bits D0 to D5).

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2.3 dbx Noise Reduction Block

All the filters required for TV-dbx Noise Reduction are incorporated. These filter responses are adjusted by setting all the FILTER SETTING bits (Write register, subaddress 02H, bits D0 to D5).

(1) LPF

This LPF has traps at f_H and 24 kHz each. The f_H trap filter minimizes interference by the f_H signal which is not synchronized with the pilot signal (for example, leakage of the synchronous idle and buzz from the video signal).

(2) 408-Hz LPF

This filter is a de-emphasis filter. Its transfer function is as follows:

$$T(f) = \frac{1 + j\frac{f}{5.23k}}{1 + j\frac{f}{408}}$$

(3) Variable Emphasis

It is also called the spectral VCA. It is controlled by the spectral RMS. The transfer function is as follows:

$$S^{-1}(f, b) = \frac{1 + j\frac{f}{20.1k} \times \frac{1 + 51b}{b + 1}}{1 + j\frac{f}{20.1k} \times \frac{1 + 51}{b + 1}}$$

where “b” is the variable transferred from the spectral RMS for controlling.

(4) Wide-band VCA

A VCA whose operating frequency range is mainly low to mid frequencies and controlled by the wide-band RMS. The transfer function is as follows:

$$W^{-1}(a) = a$$

where “a” is the variable transferred from the wide-band RMS for controlling.

(5) 2.19-kHz LPF

This filter is a de-emphasis filter. Its transfer function is as follows:

$$T(f) = \frac{1 + j\frac{f}{62.5k}}{1 + j\frac{f}{2.19k}}$$

(6) Spectral RMS Filter

A filter that limits the band width of the signal input to the RMS which controls the variable emphasis. The transfer function is as follows:

$$T(f) = \frac{\left(j\frac{f}{7.66k}\right)^2}{1 + j\frac{f}{7.31k} + \left(j\frac{f}{7.66k}\right)^2} \times \frac{j\frac{f}{3.92k}}{1 + j\frac{f}{3.92k}}$$

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(7) Wide-band RMS Filter

A filter that limits the band width of the signal input to the wide-band RMS which controls the wide-band VCA. The transfer function is as follows:

$$T(f) = \frac{1}{1 + j\dfrac{f}{2.09k}}$$

(8) Spectral RMS

Detects the RMS value of the signal passed through the spectral RMS filter, and converts the signal to the DC voltage. The release time is set by adjusting the current I_T of the μPC1851B and the capacitance of the external capacitor connected to the STI pin. The current I_T is adjusted by adjusting the current from the ITI pin.

(9) Wide-band RMS

Detects the RMS value of the signal passed through the wide-band RMS filter, and converts the signal to the DC voltage. The release time is set by adjusting the current I_T of the μPC1851B and the capacitance of the external capacitor connected to the WTI pin. The current I_T is adjusted by adjusting the current from the ITI pin.

2.4 Matrix Block

(1) Matrix

Adds L+R signal and L–R signal to output L signal, and substracts L+R signal from L–R signal to output R signal.

(2) Mode Selector

The matrix block selects the signal from the monaural signal, Stereo signal, SAP signal by the User Mode.

2.5 Selector Block

It selects the signal from the TV signal (signal with the audio multiple signal processed in the μPC1851B) and external input (signal input from EL1, EL2, ER1 and ER2 pins), and outputs it to the surround processor block (surround, tone control, and volume control block).

It also selects the gain of the selection signal (0 dB/6 dB) as well as switches the stereo/monaural output (by the I^2C bus).

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3. I²C BUS INTERFACE

The μPC1851B uses a 2-wire serial bus developed by Philips. The serial clock line (SCL) and serial data line (SDA) employ the 2-wire configuration as shown in Figure 3-1.

The μPC1851B contains an I²C bus interface circuit, eleven (8-bit) read/write registers, and one read-only register.

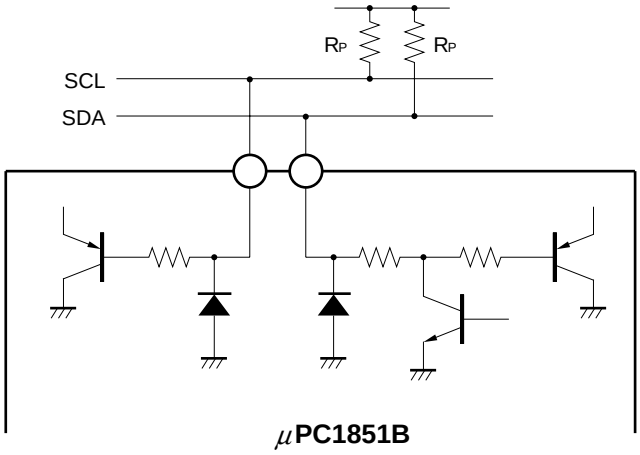
Serial Clock Line (SCL)

The master CPU outputs a serial clock to achieve data synchronicity. The μPC1851B receives serial data based on this clock. The input level is CMOS-compatible. The clock frequency is from 0 to 100 kHz.

Serial Data Line (SDA)

The master CPU outputs data synchronously with the serial clock. The μPC1851B receives this data based on the serial clock. The input level is CMOS-compatible

Figure 3-1. Internal Equivalent Circuit of Interface Pins



For SCL and SDA pins, a protection diode on the V_{CC} side is deleted not so as to pull the voltage of I²C bus line down to 0 V while the power supply is off (V_{CC} = 0 V).

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3.1 Data Transfer

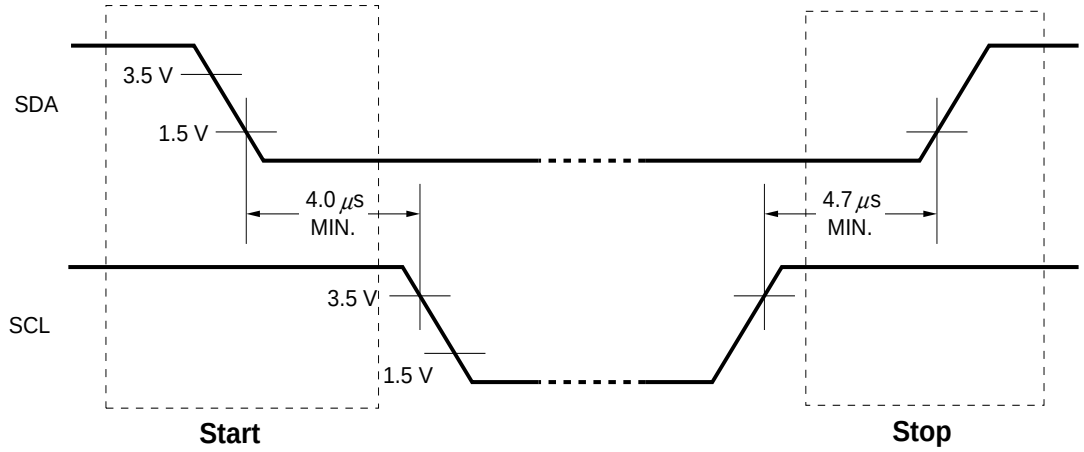
(1) Start condition

The start condition is created when SDA changes from high to low while SCL is high, as shown in Figure 3-2. When the μPC1851B receives this information, it captures data sent in synchronization with the clock.

(2) Stop condition

The stop condition is created when SDA changes from low to high while SCL is high, as shown in Figure 3-2. When the μPC1851B receives this information, it stops receiving or outputting data.

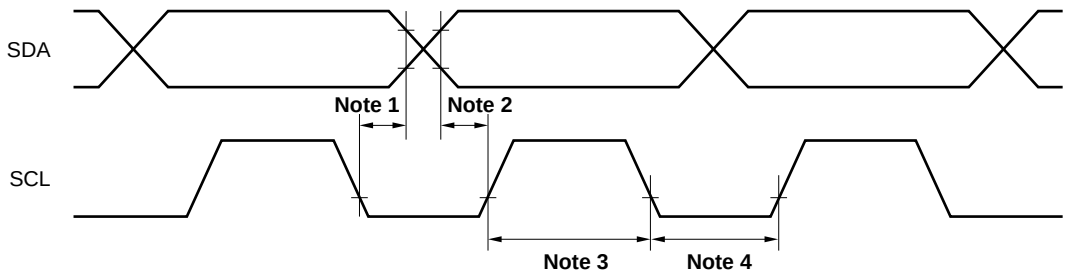
Figure 3-2. Data Transfer Start/Stop Condition



(3) Data transfer

When transferring data, be sure to switch data only when SCL is low, as shown in Figure 3-3. When SCL is high, the data must not be changed.

★ **Figure 3-3. Data Transfer**



Notes
1. Data hold time: 300 ns MIN.
2. Data setup time: 250 ns MIN.
3. Interval when data must not be changed.
4. Interval when data can be changed.

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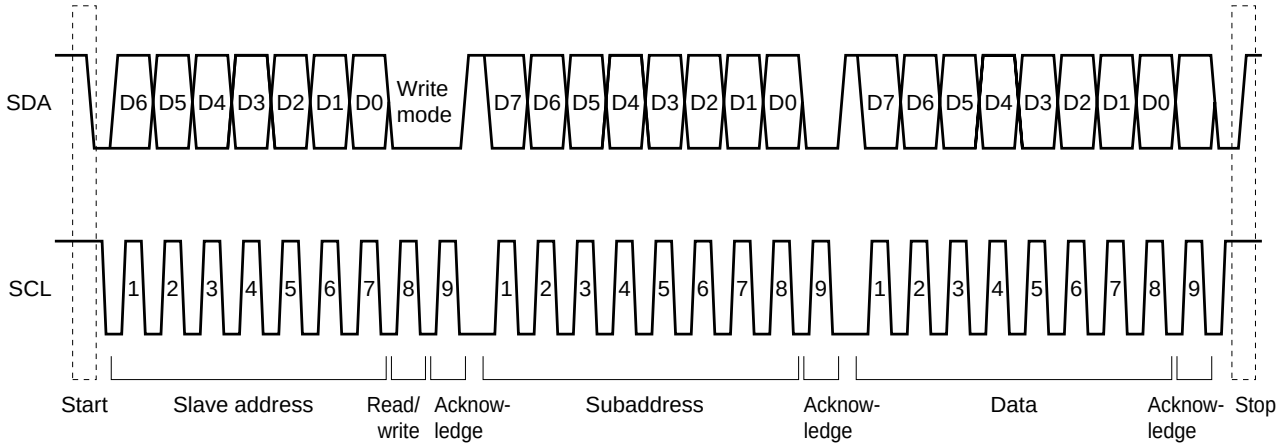
3.2 Data Transfer Format

An example of data transfer in the write mode is shown in Figure 3-4.

Figure 3-4. Data Transfer Example in Write Mode



Data consists of 8-bit units. This 8-bit data must always be followed by an acknowledge bit. Data transfer must be done on an MSB-first basis.

The first byte after a start condition specifies the slave address. The slave address consists of 7 bits.

Table 3-1 shows the slave addresses of the μPC1851B. These slave addresses are registered by Philips.

Table 3-1. Slave Addresses of μPC1851B

Slave address / Mode	D6	D5	D4	D3	D2	D1	D0	Read/Write
Write	1	0	1	1	0	0	0	0
Read	1	0	1	1	0	0	0	1

The bit following the slave address is the read/write bit specifying the direction of the data to be transferred.

During the read operation, data is transferred from the μPC1851B to the master CPU. During the write operation, data is transferred from the master CPU to the μPC1851B. “0” and “1” are written to the READ/WRITE bit during the Write and Read modes, respectively.

The byte following the slave address is the subaddress of the μPC1851B in the write mode.

The μPC1851B has eleven subaddresses, SA_0 to SA_A, which are made up of 8 bits. Following the subaddress byte is the data to be set to the subaddress.

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(1) 1-byte data transfer

The format for 1-byte data transfer is the following:

Start	Slave address	Write mode	Acknow -ledge	Subaddress	Acknow -ledge	Data	Acknow -ledge	Stop

(2) Continuous data transfer

The format when transferring multiple (7) bytes of data at one time by using the automatic increment function is the following:

Start	Slave address	Write mode	Acknow -ledge	Subaddress	Acknow -ledge	Data1	Acknow -ledge	Data2	Acknow -ledge	----------	Data7	Acknow -ledge	Stop

The master CPU transfers “00H” as subaddress SA_0 following the start condition and slave address. After the subaddress SA_0, the master CPU transfers the SA_0 data, and continues with SA_1, SA_2,..., SA_A data without transferring stop conditions in between. Finally, the stop condition is transferred and the transfer is completed.

(3) Data read

The μPC1851B has one read register. The contents of this register can be read by the master CPU.

The format when data is read is the following:

Start	Slave address	Read	Acknow -ledge	Data	Non- acknow -ledge	Stop

(4) Acknowledge

In the case of the I^2C bus, an acknowledge bit is added to the data as the 9th bit to determine whether data transfer was successful. The master CPU determines the success or failure of data transfer based on whether this acknowledge bit is a logical low or high.

If the acknowledge interval is a logical low, this indicates that data transfer was successful. If it is a logical high, this indicates that data transfer was unsuccessful or that the slave side forcibly released the bus.

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(5) Automatic increment

The μPC1851B has the automatic increment function.

The automatic increment is applied to the subaddresses 00H to 05H of the write register.

The user can set ON/OFF the automatic increment of the subaddresses 06H to 0AH (refer to **4.1 Subaddress List**).

Automatic increment ON: The subaddress is automatically increased. Setting the slave address and subaddress once enables the data of the next subaddress to be transferred without actually setting it.

Automatic increment OFF: The subaddress is fixed. The data of the fixed subaddress can be set time after time.

The increment of the subaddresses 06H to 0AH is individually controlled by each automatic increment ON/OFF bit.

For example, if the automatic increment function of the subaddress 06H is set to ON and that of the subaddress 07H set to OFF, the subaddress is to be automatically increased from 06H to 07H and then fixed to 07H.

Though the automatic increment function of the subaddress 0AH is set to ON, the subaddress is not to be increased. After setting the data of 0AH (acknowledge bit: low level), if the next data is transferred, the acknowledge is to be in non-acknowledge state (acknowledge bit: high level) and the data transfer from the master CPU is aborted.

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4. I²C BUS COMMANDS

4.1 Subaddress List

(1) Write register (command list)

Bit / Sub-address	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	0	During noise detection Stereo/SAP output stop 0: SAP OFF 1: Stereo, SAP OFF	Input level setting					
01H	0	f_H monitor ON/OFF 0: OFF 1: ON	Stereo VCO setting					
02H	0	Pilot canceler ON/OFF 0: ON 1: OFF	Filter setting					
03H	0	Input gain 0: 0 dB 1: 6 dB	Low-band separation setting					
04H	0	Surround 0: OFF 1: ON	High-band separation setting					
05H	0	$5f_H$ monitor ON/OFF 0: OFF 1: ON	SAP VCO setting					
06H	Automatic increment 0: OFF 1: ON	Input select 1 00: TV signal 01: External input 1 10: External input 2 11: Setting prohibited		Input select 2 0: Stereo 1: Monaural	SAP1/SAP2 switch[Note] 0: SAP1 1: SAP2	Stereo/SAP switch 0: Stereo 1: SAP	Forced monaural 0: OFF 1: ON	Mute 0: ON 1: OFF
07H	0	Automatic increment 0: OFF 1: ON	Volume control					
08H	0	Automatic increment 0: OFF 1: ON	Balance control					
09H	0	Automatic increment 0: OFF 1: ON	Bass control					
0AH	0	Automatic increment 0: OFF 1: ON	Treble control					

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Note Output when SAP1 or SAP2 is selectd is as follows:

	L-channel output (LOT pin)	R-channel output (ROT pin)
SAP1	SAP	
SAP2	Monaural (L+R)	SAP

(2) Read register

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
	Broadcast status			Reception status			
Power-on reset	Stereo pilot	SAP signal	Noise detection	Stereo broadcast reception	SAP broadcast reception	1	1
——	0: Not available	0: Not available	0: Not available	0: Not available	0: Not available		
1: Detect	1: Available	1: Available	1: Available	1: Available	1: Available		

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4.2 Setting Procedure

Precise adjustment of the dbx decoder is absolutely critical for optimum performance. Where possible, the adjustment should be performed after the μPC1851B is mounted on the chassis and with the video system active.

Set the data of write register as follows before the adjustment.

Table 4-1. Default Setting of Write Register

Bit / Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	1	0	0	0	0	0
01H	0	0	1	0	0	0	0	0
02H	0	0	1	1	1	1	1	1
03H	0	0	1	0	0	0	0	0
04H	0	0	1	0	0	0	0	0
05H	0	0	1	0	0	0	0	0
06H	0	0	0	0	0	0	0	1
07H	0	1	1	1	1	1	1	1
08H	0	1	1	0	0	0	0	0
09H	0	1	1	0	0	0	0	0
0AH	0	1	1	0	0	0	0	0

(1) Input level setting (Write register, subaddress 00H, bits D5 to D0)

<1> Write “1” to bit D0 (Mute: OFF) of subaddress 06H.

<2> Input sine wave of 300 Hz, 150 mV_{rms} to COM pin.

<3> Set bits D5 to D0 (INPUT LEVEL SETTING bits) of subaddress 00H so that the output level of FOR pin is 500 mV_{rms} (±10 mV_{rms}).

(2) Stereo VCO setting (Write register, subaddress 01H, bits D6 to D0)

Perform this adjustment with no signal applied.

<1> Write “1” to bit D0 (Mute: OFF) of subaddress 06H.

<2> Write “1” to bit D6 (f_H monitor: ON) of subaddress 01H.

<3> Connect frequency counter to FOR pin, and set bits D5 to D0 (STEREO VCO SETTING bits) of subaddress 01H so that frequency counter displays 15.73 kHz (±0.1 kHz).

<4> When setting is completed, write “0” to bit D6 (f_H monitor: OFF) of subaddress 01H.

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(3) Filter setting (Write register, subaddress 02H, bits D6 to D0)

<1> Write “1” to bit D6 (Pilot canceler: OFF) of subaddress 02H.
<2> Input pilot signal (15.734 kHz, 30 mVrms or higher **Note**) to COM pin and set data of bits D5 to D0 (FILTER SETTING bits) of subaddress 02H so that the AC output level of the FOR pin becomes as small as possible (Decrease the set data from 63 (decimal)).
<3> When setting is completed, write “0” to bit D6 (pilot canceler: ON) of subaddress 02H.

Note Recommended 100 mVrms.

(4) Separation setting (Write register, subaddresses 03H and 04H, bits D5 to D0)

<1> Write “1” to bit D0 (Mute: OFF) of subaddress 06H.
<2> Write “20H” to bits D5 to D0 (HIGH-BAND SEPARATION SETTING bits) of subaddress 04H.
<3> Input composite signal to COM pin (300 Hz, 30 % modulation, L-only, with noise reduction), and set bits D5 to D0 (LOW-BAND SEPARATION SETTING bits) of subaddress 03H so that the output level of the FOR pin is as small as possible.
<4> Change the modulation frequency of the composite signal to 3 kHz, and set bits D5 to D0 of subaddress 04H so that the output level of the FOR pin is as small as possible.
<5> While bits D5 to D0 of subaddress 04H are set as in step <4> above, repeat the setting procedure of step <3> for bits D5 to D0 of subaddress 03H.

(5) SAP VCO setting (Write register, subaddress 05H, bits D6 to D0)

Perform this adjustment with no signal applied.

<1> Add a 1 MΩ resistor between the SOA pin and GND.
<2> Write “1” to bit D0 (Mute: OFF) of subaddress 06H.
<3> Write “1” to bit D6 (5 f_H monitor: ON) of subaddress 05H.
<4> Connect a frequency counter to the FOR pin, and set bits D5 to D0 of subaddress 05H (SAP VCO SETTING bits) so that 78.67 kHz (±0.5 kHz) is displayed on the frequency counter.
<5> When setting is completed, write “0” to bit D6 (5 f_H monitor: OFF) of subaddress 05H.
<6> Delete the 1 MΩ resistor between the SOA pin and GND.

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4.3 Explanation of Write Register

(1) Stereo/SAP output stop function during noise detection

Stereo/SAP output stop can be selected with the data of bit D6 of subaddress 00H during weak electrical field conditions (recommended noise level during circuit use is 34 mVrms (TYP.) or more).

SAP output stop : Only SAP output is stopped.
SAP and stereo output stop : SAP and stereo outputs are stopped, switch to monaural output.

Noise level detection is performed, when detected a noise about at 11.5 f_H (180 kHz), a frequency that is sufficiently apart from that of the high frequency signals such as the stereo, SAP, and telemetry signal. If noise is detected, "1" is set to bit D4 of the read register (Refer to section **4.4, (4) Noise detection**)

Figure 4-1. Stereo/SAP Output Stop Function During Noise Detection

	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	During noise detection	Input level setting					

Stereo/SAP output stop function during noise detection

0	SAP output stop
1	SAP and stereo output stop

(2) Mute

The mute function can be set ON/OFF with the data of bit D0 of subaddress 06H.
The mute on state is entered when bit D0 is set to 0 after power-on reset.

Figure 4-2. Mute

	D7	D6	D5	D4	D3	D2	D1	D0
06H	Automatic increment	Input select 1		Input select 2	SAP1/SAP2 switch	Stereo/SAP switch	Forced monaural ON/OFF	Mute ON/OFF

Mute

0	Mute ON
1	Mute OFF

Caution When switching the power ON/OFF, use the external mute (200 ms) in order to minimize shock noise.

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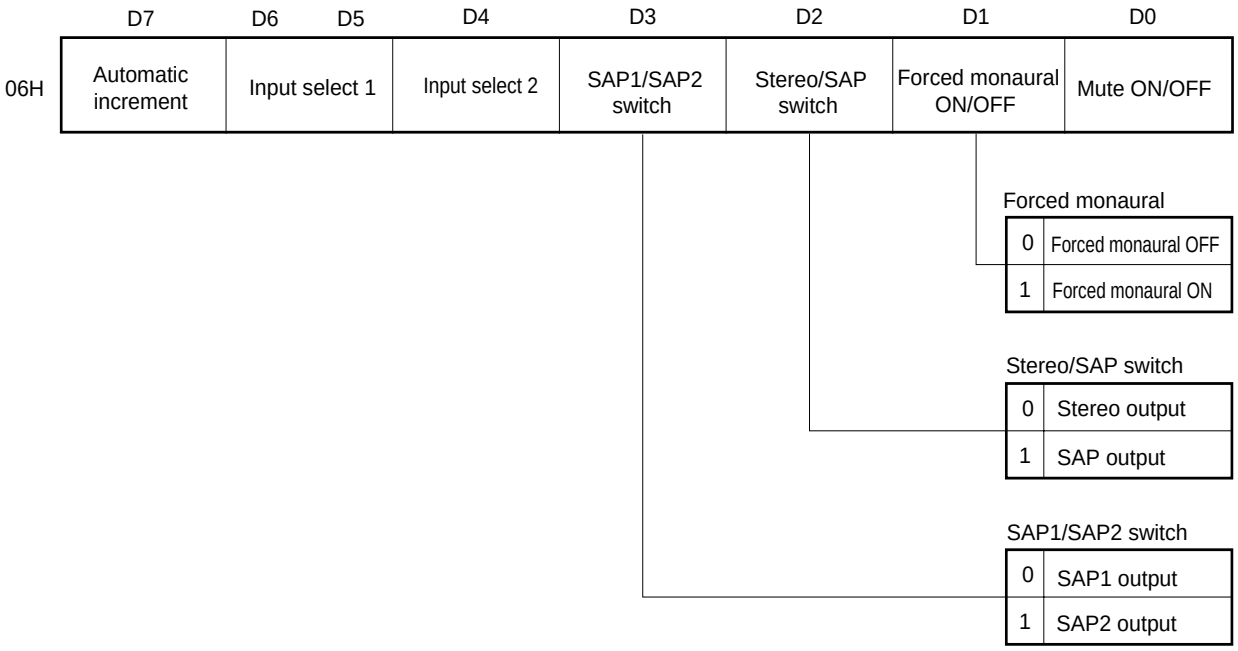
(3) Mode switch (L-, R-channel output (LOT, ROT pins))

The output signal for the L- and R-channel outputs (LOT, ROT pins) can be selected with bits D3 to D1 of subaddress 06H. For the combinations of data of each output signal bit, refer to **5. MODE MATRIX**.

Forced monaural ON/OFF : When set to ON, a monaural signal is forcibly output regardless of the selection of other bits.
Stereo/SAP switch : When forced monaural is set to OFF, performs selection of stereo or SAP.
SAP1/SAP2 switch : When SAP output is selected with the stereo/SAP switch, performs selection of SAP1 or SAP2.

	L-Channel Output (LOT pin)	R-Channel Output (ROT pin)
SAP1	SAP output	
SAP2	Monaural (L+R) output	SAP output

Figure 4-3. Mode Switch (L-, R-Channel Output (LOT, ROT pins))



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(4) Input select

The signal to be input to the selector block in the μPC1851B can be selected by the data of bits D4 to D6 of subaddress 06H. The selected signal is output from the LOT, ROT, FOL and FOR pins.

For the combination of bits for the signal to be selected, refer to **6. SELECTOR TABLE**.

Input select 1 : switches the TV signal (signal with the audio multiple signal processed in the μPC1851B) and external inputs 1 and 2 (signal input from EL1, EL2, ER1 and ER2 pins).

Input select 2 : switches the stereo signal and monaural signal.

Figure 4-4. Input Select

	D7	D6	D5	D4	D3	D2	D1	D0
06H	Automatic increment	Input select 1		Input select 2	SAP1/SAP2 switch	Stereo/SAP switch	Forced monaural ON/OFF	Mute

Input select 2

	L-channel output (LOT, FOL pins)	R-channel output (ROT, FOR pins)
0	L-channel signal	R-channel signal
1 Note	Monaural (L+R) signal	

Input select 1

00	TV signal
01	External input 1
10	External input 2
11	Setting prohibited

Note When SAP2 is selected by switching SAP1/SAP2, the L+R signal and SAP signal are composite to be output.

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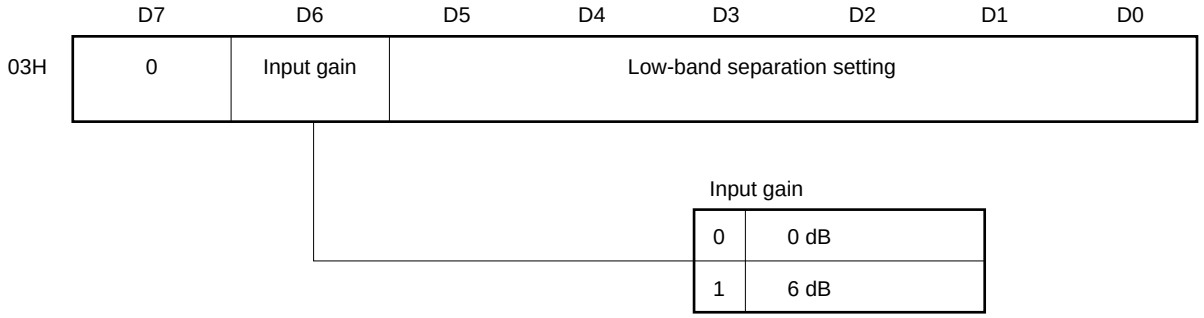
(5) Input gain

The gain of the signal to be input to the selector block in the μPC1851B can be selected by the data of bit D6 of subaddress 03H.

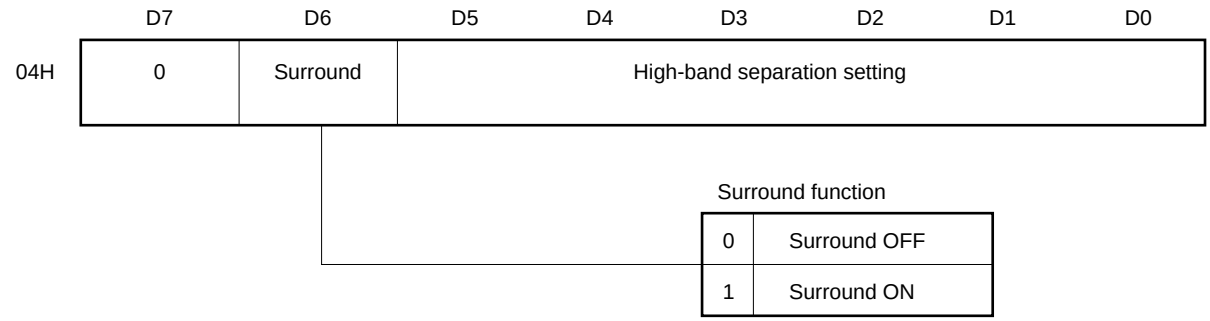
Figure 4-5. Input Gain



(6) Surround function

The surround function ON/OFF can be selected by the data of bit D6 of subaddress 04H.

Figure 4-6. Surround Function



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(7) Volume, Balance control

The volume and balance of the output (LOT and ROT pins) can be controlled at 64 levels by the data of bits D0 to D5 of subaddresses 07H and 08H.

The volume attenuation is 80 dB or higher.

Figure 4-7. Volume, Balance Control

- **Volume control**

	D7	D6	D5	D4	D3	D2	D1	D0
07H	0	Automatic increment	Volume control					

Volume control

Data D5 - D0	Attenuation volume
111111	Flat (0 dB)
|	|
000000	Low

- **Balance control**

	D7	D6	D5	D4	D3	D2	D1	D0
08H	0	Automatic increment	Balance control					

Balance control

Data D5 - D0	Attenuation volume
111111	L-ch Low, R-ch Flat
|	|
100000	TYP.
|	|
000000	L-ch Flat, R-ch Low

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(8) Bass, Treble control

The bass and treble sound quality of the output (LOT and ROT pins) can be controlled at 64 levels by the data of the bits D0 to D5 of subaddresses 09H and 0AH.

The bass control amount of the low frequency band width boost/cut is ±11 dB TYP. at 100 Hz.

The treble control amount of the high frequency band width boost/cut is ±13 dB TYP. at 10 kHz.

Figure 4-8. Bass, Treble control

- **Bass control**

	D7	D6	D5	D4	D3	D2	D1	D0
09H	0	Automatic increment	Bass control					

Bass control

Data D5 - D0	Gain
111111	Boost
|	|
100000	0 dB
|	|
000000	Cut

- **Treble control**

	D7	D6	D5	D4	D3	D2	D1	D0
0AH	0	Automatic increment	Treble control					

Treble control

Data D5 - D0	Gain
111111	Boost
|	|
100000	0 dB
|	|
000000	Cut

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(9) Automatic increment function

The automatic increment function ON/OFF can be selected by the data of bit D7 of subaddress 06H and that of bit D6 of subaddresses 07H to 0AH. For the details of the automatic increment function, refer to **3.2 (5) Automatic increment**.

Figure 4-9. Automatic Increment Function

	D7	D6	D5	D4	D3	D2	D1	D0
06H	Automatic increment	Input select 1		Input select 2	SAP1/SAP2 switch	Stereo/SAP switch	Forced monaural ON/OFF	Mute

Automatic increment function

0	Automatic increment function OFF
1	Automatic increment function ON

Caution After power-on reset, be sure to set the data.

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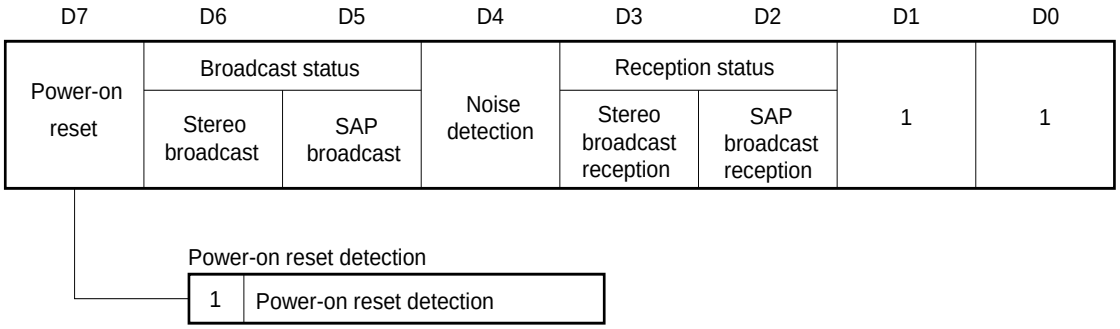
4.4 Explanation of Read Register

(1) Power-on reset detection

Whether a power-on reset was detected is detected with bit D7 of the read register.

Figure 4-10. Power-On Reset Detection

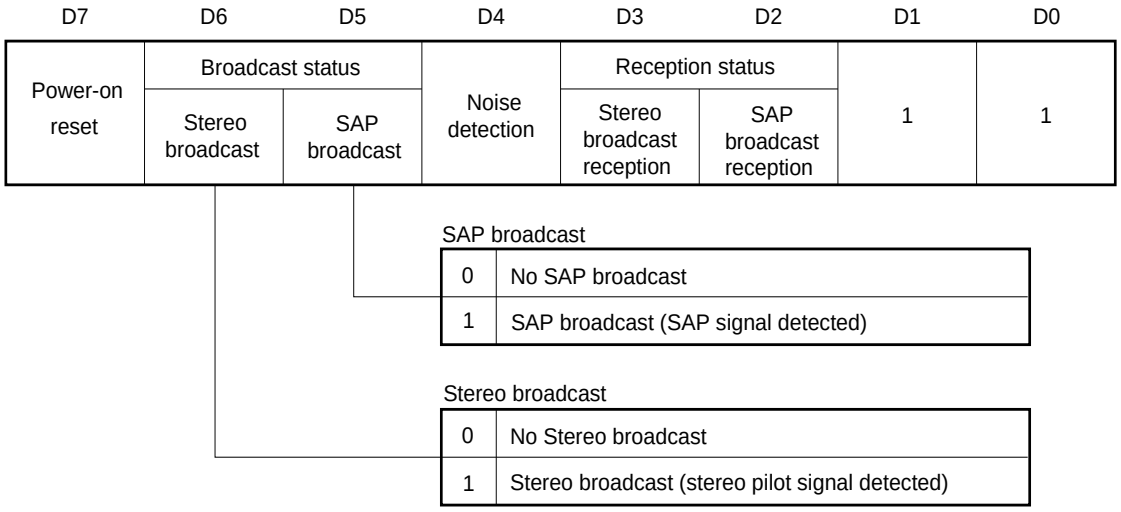


(2) Stereo, SAP broadcast (broadcast status) detection

Whether SAP or stereo broadcast from a broadcasting station is being broadcast is detected with bits D5 and D6 of the read register.

When a SAP signal (5 f_H) or stereo pilot signal is detected, the register data becomes “1”.

Figure 4-11. Stereo, SAP Broadcast (Broadcast Status) Detection



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(3) Stereo, SAP broadcast reception (reception status) detection

Whether SAP or stereo broadcast is being received and the μPC1851B outputs the audio signal can be detected with bits D2 and D3 of the read register. The register data become "1" only if the SAP signal (5 f_H) is detected when the SAP broadcast reception is selected, or if the stereo pilot signal is detected when the stereo broadcast reception is selected.

Figure 4-12. Stereo, SAP Broadcast Reception (Reception Status) Detection

D7	D6	D5	D4	D3	D2	D1	D0
Power-on reset	Broadcast status		Noise detection	Reception status		1	1
	Stereo broadcast	SAP broadcast		Stereo broadcast reception	SAP broadcast reception		

SAP broadcast reception

0	No outputing SAP broadcast
1	Outputing SAP broadcast

Stereo broadcast reception

0	No outputing stereo broadcast
1	Outputing stereo broadcast

(4) Noise detection

Noise can be detected with bit D4 of the read register. It is monitored in the vicinity of the 11.5 f_H (180 kHz) signal level.

During noise detection, the operation of the SAP demodulator block and the stereo demodulation block is interrupted (Refer to section **4.3 (1) Stereo/SAP output stop function during noise detection**).

Figure 4-13. Noise Detection

D7	D6	D5	D4	D3	D2	D1	D0
Power-on reset	Broadcast status		Noise detection	Reception status		1	1
	Stereo broadcast	SAP broadcast		Stereo broadcast reception	SAP broadcast reception		

Noise detection

0	No noise
1	Noise

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5. MODE MATRIX

Mute OFF (Write register, subaddress 06H, bit D0 : "1")

(1) Read register, bit D4: 0

Broadcast mode	Write Register				Output		Read Register			
	Forced monaural ON/OFF	Stereo /SAP switch	SAP1 /SAP2 switch	Stereo /SAP output stop	L-ch output (LOT)	R-ch output (ROT)	Broadcast status		Reception status	
							Stereo pilot	SAP signal	Stereo broadcast reception	SAP broadcast reception
	Subaddress 06H			Subaddress 00H						
	Bit D1	Bit D2	Bit D3	Bit D6			Bit D6	Bit D5	Bit D3	Bit D2
Monaural	–	–	–	–	L+R		0	0	0	0
Stereo	0	–	–	–	L	R	1	0	1	0
	1				L+R				0	
Monaural+SAP	0	0	–	–	L+R		0	1	0	0
		1	0		SAP					1
			1		L+R	SAP				
	1	–	–		L+R					0
Stereo+SAP	0	0	–	–	L	R	1	1	1	0
		1	0		SAP				0	1
			1		L+R	SAP				
	1	–	–		L+R					0

(2) Read register, bit D4: 1

Broadcast mode	Write Register				Output		Read Register			
	Forced monaural ON/OFF	Stereo /SAP switch	SAP1 /SAP2 switch	Stereo /SAP output stop	L-ch outputl (LOT)	R-ch output (ROT)	Broadcast status		Reception status	
							Stereo pilot	SAP signal	Stereo broadcast reception	SAP broadcast reception
	Subaddress 06H			Subaddress 00H						
	Bit D1	Bit D2	Bit D3	Bit D6			Bit D6	Bit D5	Bit D3	Bit D2
Monaural	–	–	–	–	L+R		0	0	0	0
Stereo	0	–	–	0	L	R	1	0	1	0
				1	L+R		0		0	
Monaural+SAP	0	1	0	0	L+R		0	0	0	0
				1						
			1	0						
				1						
Stereo+SAP	0	0	–	0	L	R	1	0	1	0
				1	L+R		0		0	
		1	0	0						
				1						
			1	0						
				1						

Remarks 1. When the μPC1851B recognizes a weak electric field, bit D4 of the read register becomes "1".

2. —: Don't care.

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6. SELECTOR TABLE

Input signal:

TV signal (signal with the audio multiple signal processed in the μPC1851B) L-channel, R-channel
External input 1 (signal input from EL1, ER1 pins) L-channel, R-channel
External input 2 (signal input from EL2, ER2 pins) L-channel, R-channel

Write Register			Output	
Mute ON/OFF	Input select 1	Input select 2	L-channel output (LOT, FOL pins)	R-channel output (ROT, FOR pins)
Subaddress : 06H				
Bit : D0	Bits : D6, D5	Bit : D4		
0	– –	–	Mute	
1	00	0	TV signal (L)	TV signal (R)
	01		External input 1 (L)	External input 1 (R)
	10		External input 2 (L)	External input 2 (R)
	11		Setting prohibited (no signal, unconnected)	
	00	1	TV signal	$\frac{1}{2}$ (L+R)
	01		External input 1	$\frac{1}{2}$ (L+R)
	10		External input 2	$\frac{1}{2}$ (L+R)
	11		Setting prohibited (no signal, unconnected)	

Remark – : Don't care

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7. USAGE CAUTIONS

7.1 Caution on Shock Noise Reduction

When switching the power ON/OFF, use the external mute (approx. 200 ms) in order to minimize shock noise (Refer to section **4.3 (2) Mute**).

7.2 Supply Voltage

Pass data through the I²C bus only after stabilizing the supply voltage of the entire application system.

7.3 Impedance of Input and Output Pins

Table 7-1. Impedance of Input and Output Pins

Input pin		
Symbol	Description	Impedance
COM	Composite signal input	80 kΩ
SI	SAP single input	
EL1, EL2	External L-channel input	
ER1, ER2	External R-channel input	

Output pin		
Symbol	Description	Impedance
SOT	SAP single input	360 Ω
ROT	R-channel output	15 Ω
LOT	L-channel output	
MOR	R-channel matrix output	
MOL	L-channel matrix output	
FOR	R-channel fixed output	
FOL	L-channel fixed output	

7.4 Drive Capability of Output Pins

Table 7-2. Drive Capability of Output Pins

Pin symbol	Pin description	Output pin-GND Connection Resistance	Drive capability
SOT	SAP single output	10 kΩ	3-kΩ load or less
ROT	R-channel output		700-Ω load or less
LOT	L-channel output		
MOR	R-channel matrix output		
MOL	L-channel matrix output		
FOR	R-channel fixed output		
FOL	L-channel fixed output		

Remark If the load capacitance of the output pins (SOT, ROT, LOT, MOR, MOL, FOR, FOL pins) exceeds 100 pF, parasitic oscillation may occur. In this case, connect a resistor between the output pins and the load capacitance. Bear in mind that the load capacitance is changed by wiring pattern on the printed circuit board.

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7.5 Caution on External Components

According to the license contract with THAT Corporation, use the following for external components.

★ With regard to the use of other external components, please contact to THAT corporation.

Table 7-3. External Components

Pin symbol	Pin description	External component
ITI	Timing current setting	Metal film resistor (±1 %)
STI	Spectral RMS timing	Tantalum capacitor (±10 %)
WTI	Wide-band RMS timing	

7.6 Change of Electrical Characteristics by External Components

(1) SAP sensitivity can be lowered by inserting a resistor between the SDT pin and GND.

(2) Noise sensitivity can be changed by changing the value of the resistor between the NDT pin and GND.

(3) The capture range can be changed by changing the recommended 1 μF value of the capacitor between the φD1 and φD2 pins.
Reducing the capacitor value increases the capture range, and increasing it reduces the capture range. However, too small a capacitor value may cause the distortion rate to become worse during stereo output, or may cause malfunction. In this case, please contact NEC.

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8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}	V_{CC} pin	11.0	V
I^2C bus input pin voltage	V_{cont}	SDA, SCL pins	V_{CC}	V
Composite signal input voltage	V_{in}	COM pin	V_{CC}	V
Package power dissipation	P_D		700	mW
Operating ambient temperature	T_A	V_{CC} = 9 V	–20 to +75	°C
Storage temperature	T_{stg}		–40 to +125	°C

Caution Exposure to Absolute Maximum Rating for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

Recommended Operating Conditions (unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{CC}	V_{CC} pin		8.0	9.0	10.0	V
I^2C bus input pin voltage (High level)	$V_{cont(H)}$	SDA, SCL pins		3.5	–	5.0	V
I^2C bus input pin voltage (Low level)	$V_{cont(L)}$			0	–	1.5	V
Input impedance	R_{in}	COM, SI, EL1, EL2, ER1, ER2 pins		60	–	95	kΩ
Output load impedance 1	R_{L1}	LOT, ROT, MOL, MOR, FOL, FOR pins, AC load impedance at 100 % modulation		2.0	–	–	kΩ
Output load impedance 2	R_{L2}	SOT pin, AC load impedance at 100 % modulation		10.0	–	–	kΩ
Output load impedance 3	R_{L3}	LOT, ROT, MOL, MOR, FOL, FOR pins, DC load impedance at 100 % modulation		5.0	–	–	kΩ
Output load impedance 4	R_{L4}	SOT pin, DC load impedance at 100 % modulation		25.0	–	–	kΩ
Composite signal input voltage	V_{in}	COM pin	L+R signal, 100 % modulation	–	0.424	–	V_{p-p}
			L–R signal, 100 % modulation	–	0.848	–	V_{p-p}
			Pilot signal	–	0.0848	–	V_{p-p}
			SAP signal	–	0.254	–	V_{p-p}
External input signal voltage	V_{ext}	EL1, EL2, ER1, ER2 pins		–	1.4	5.6	V_{p-p}
Clock frequency	f_{SCL}	SCL pin		–	–	100	kHz

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Electrical Characteristics
(unless otherwise specified, T_A = 25 °C, RH ≤ 70 %, V_{CC} = 9.0 V, adding 30 kHz LPF to output pins)

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input: COM pin, Output: FOL, FOR pins						
Supply current	I_{CC}	No signal	–	57	75	mA
Stereo detection input sensitivity	ST_{SENCE}	15.734 kHz, sine wave	11	16	21	mV_{rms}
Stereo detection hysteresis	ST_{HY}	Only stereo pilot signal input	5.0	5.7	10	dB
Stereo detection capture range	ST_{CCL}	Vin = 30 mVrms	–5.5	–4.0	–2.5	%
	ST_{CCH}	Only stereo pilot signal input	+2.5	+4.0	+5.5	%
SAP detection input sensitivity	SAP_{SENCE}	f = 78.67 kHz, 0% modulation	17	23	30	mV_{rms}
SAP detection hysteresis	SAP_{HY}	Only SAP carrier input	3.3	4.8	6.3	dB
Noise detection input sensitivity	NO_{SENCE}	Input sine wave f: Noise BPF peak	20	30	40	mV_{rms}
Noise detection hysteresis	NO_{HY}	Input sine wave f: Noise BPF peak	1	2	3	dB
Monaural total output voltage	V_{OMO}	300 Hz, 100% modulation, Pre-emphasis: ON	480	500	520	mV_{rm}
Stereo total output voltage	V_{OST}	300 Hz, 100 % modulation	450	500	550	mV_{rms}
SAP total output voltage	V_{OSAP1}	Noise reduction: ON	400	500	600	mV_{rms}
Difference between monaural L and R output voltage	V_{OLR}	300 Hz, 100% modulation	–0.5	–	+0.5	dB
Monaural total frequency characteristics 1	V_{OMO1}	1 kHz, 30% modulation, (f = 300 Hz: 0 dB) Pre-emphasis: ON	–0.5	–	+0.5	dB
Monaural total frequency characteristics 2	V_{OMO2}	3 kHz, 30% modulation, (f = 300 Hz: 0 dB) Pre-emphasis: ON	–0.5	–	+0.5	dB
Monaural total frequency characteristics 3	V_{OMO3}	8 kHz, 30% modulation, (f = 300 Hz: 0 dB) Pre-emphasis: ON	–0.8	–	+0.8	dB
Monaural total frequency characteristics 4	V_{OMO4}	12 kHz, 30% modulation, (f = 300 Hz: 0 dB) Pre-emphasis: ON	–5.5	–3.0	–1.5	dB
Stereo total frequency characteristics 1	V_{OST1}	1 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–0.5	–	+0.5	dB
Stereo total frequency characteristics 2	V_{OST2}	3 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–0.5	–	+0.5	dB
Stereo total frequency characteristics 3	V_{OST3}	8 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–1.0	–	+1.0	dB
Stereo total frequency characteristics 4	V_{OST4}	12 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–8.0	–5.0	–2.0	dB
SAP total frequency characteristics 1	V_{OSAP11}	1 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–1.2	+0.3	+1.2	dB
SAP total frequency characteristics 2	V_{OSAP12}	3 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–1.2	0.0	+1.2	dB
SAP total frequency characteristics 3	V_{OSAP13}	8 kHz, 30% modulation, (f = 300 Hz: 0 dB) Noise reduction: ON	–4.0	–1.0	+1.0	dB
Stereo channel separation 1	Sep_1	300 Hz, 30% modulation	27	32	–	dB

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Stereo channel separation 2	Sep_2	1 kHz, 30% modulation	23	30	–	dB
Stereo channel separation 3	Sep_3	3 kHz, 30% modulation	27	35	–	dB
Stereo channel separation 4	Sep_4	5 kHz, 30 % modulation	23	30	–	dB
Stereo channel separation 5	Sep_5	8 kHz, 30 % modulation	–	25	–	dB
Monaural total harmonic distortion	THD_{MO}	1 kHz, 100% modulation Pre-emphasis: ON	–	0.1	0.5	%
Stereo total harmonic distortion 1	THD_{ST1}	1 kHz, 100% modulation Noise reduction: ON	–	0.3	1.5	%
Stereo total harmonic distortion 2	THD_{ST2}	8 kHz, 30% modulation Noise reduction: ON	–	0.8	1.8	%
SAP total harmonic distortion	THD_{SAP}	1 kHz, 100% modulation Noise reduction: ON	–	0.5	2.0	%
Crosstalk 1 (SAP → Stereo)	CT_1	SAP : 1 kHz, 100 % modulation Stereo : Pilot signal only, 0 % modulation Filter: 1 kHz BPF User mode: Stereo	–	–	–65	dB
Crosstalk 2 (Stereo → SAP)	CT_2	Stereo : 1 kHz, 100 % modulation, SAP : Carrier only, 0 % modulation Filter: 1 kHz BPF User mode: SAP1	–	–	–65	dB
Monaural total S/N	S/N_{MO}	300 Hz, 100% modulation Pre-emphasis: ON	65	68	–	dB
Stereo total S/N	S/N_{ST}	300 Hz, 100 % modulation	60	65	–	dB
SAP total S/N	S/N_{SAP}	Noise reduction: ON	70	80	–	dB
Input: External input pins, output: LOT, ROT pins						
Total muting level	Mute	TV signal : 1 kHz, 100 % modulation External input : 1 kHz, 500 mV_{rms}	80	–	–	dB
Timing current	I_T	Current provided to STI and WTI pins	7.1	7.5	7.9	μA
Inter-mode DC offset 1	V_{DOF1}	Mute → Monaural	–50	–	+50	mV
Inter-mode DC offset 2	V_{DOF2}	Mute → Stereo	–50	–	+50	mV
Inter-mode DC offset 3	V_{DOF3}	Mute → SAP1	–50	–	+50	mV
Inter-mode DC offset 4	V_{DOF4}	Mute → External input	–50	–	+50	mV
Surround output characteristics 1	V_{SR1L}	External L-channel input : 100 Hz, 150 mV_{rms} Surround : ON, LOT pin	–7.5	–4.5	0.0	dB
Surround output characteristics 2	V_{SR2L}	External L-channel input : 1 kHz, 150 mV_{rms} Surround : ON, LOT pin	4.0	5.6	7.0	dB
Surround output characteristics 3	V_{SR3L}	External L-channel input : 10 kHz, 150 mV_{rms} Surround : ON, LOT pin	4.5	–	8.0	dB
Surround output characteristics 4	V_{SR4R}	External L-channel input : 1 kHz, 150 mV_{rms} Surround : ON, ROT pin	–1.5	–	+1.5	dB

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Parameter	Symbol	Conditions	Sub-address	Data	MIN.	TYP.	MAX.	Unit
Low frequency band width boost control	V_{BB}	100 Hz,	09H	3FH	9	11	13	dB
Low frequency band width cut control	V_{BC}	External input = 150 mV_{rms}		00H	–13	–11	–9	dB
High frequency band width boost control	V_{TB}	10 kHz,	0AH	3FH	10	13	16	dB
High frequency band width cut control	V_{TC}	External input = 150 mV_{rms}		00H	–16	–13	–10	dB
Volume attenuation 1	ATT_{VL1}	1 kHz,	07H	3FH	–1.0	0.0	+1.0	dB
Volume attenuation 2	ATT_{VL2}	External input = 500 mV_{rms}		20H	–20	–17.5	–14	dB
Volume attenuation 3	ATT_{VL3}			00H	–	–	–80	dB
Balance attenuation L-ch 1	ATT_{BL1}	1 kHz,	08H	3FH	–	–	–60	dB
Balance attenuation L-ch 2	ATT_{BL2}	External input = 500 mV_{rms}		30H	–14	–10	–6	dB
Balance attenuation L-ch 3	ATT_{BL3}			20H	–1.0	0.0	+1.0	dB
Balance attenuation L-ch 4	ATT_{BL4}			00H	–1.0	0.0	+1.0	dB
Balance attenuation R-ch 1	ATT_{BR1}			3FH	–1.0	0.0	+1.0	dB
Balance attenuation R-ch 2	ATT_{BR2}			20H	–1.0	0.0	+1.0	dB
Balance attenuation R-ch 3	ATT_{BR3}			10H	–14	–10	–6	dB
Balance attenuation R-ch 4	ATT_{BR4}			00H	–	–	–60	dB
Difference between monaural L and R output voltage 1 (in case of external input)	V_{OLR1}	1 kHz, External input = 500 mV_{rms}	07H	3FH	–1.5	0.0	+1.5	dB
Difference between monaural L and R output voltage 2 (in case of external input)	V_{OLR2}			20H	–2.0	0.0	+2.0	dB
Difference between monaural L and R output voltage 3 (in case of external input)	V_{OLR3}			10H	–3.0	0.0	+3.0	dB
Crosstalk 3 TV signal → External input	CT_3	TV signal: 1 kHz, 100 % modulation	07H	3FH	–	–	–80	dB
Crosstalk 4 L-ch → R-ch	CT_4	External input: 1 kHz, 500 mV_{rms}			–	–80	–70	dB
Total harmonic distortion (in case of external input)	THD_{EXT}	1 kHz, External input = 500 mV_{rms}	07H	3FH	–	0.1	0.5	%
Maximum input voltage of external input	V_{IEM}	1 kHz, Total harmonic distortion rate: 1 % (External input)	07H	3FH	1.7	2.1	–	V_{rms}
Output noise (in case of external input)	NO	No signal, R_g = 600 Ω, Filter: DIN/AUDIO	07H	3FH	–	50	150	μV_{rms}

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Test Condition Parameters for Electrical Characteristics

(Unless otherwise specified, T_A = 25 °C, RH ≤ 70 %, V_{CC} = 9 V, adding 30 kHz LPF to output pins)

Parameter	Symbol	Test Conditions	User Mode Note
Supply current	I_{CC}	I_{CC} : Current sent to V_{CC} pin when there is no signal	Monaural
Stereo detection input sensitivity	ST_{SENCE}	ST_{SENCE} : Input signal level of COM pin (input signal: 15.734 kHz) When read register D6 changes from 0 to 1	Stereo
Stereo detection hysteresis	ST_{HY}	ST_{HY} =20 log (ST_{SENCE} ÷ V) ST_{SENCE}: Stereo detection input sensitivity V: Input signal level of COM pin (Input signal: 15.734 kHz) Read register D6 is first set to 1, then input signal level is gradually lowered until D6 is changed to 0	
Stereo detection capture range	ST_{CCL}	ST_{CCL} = Δf ÷ 15.734 kHz Δf: Difference between f and 15.734 kHz f: Input signal (14.5 kHz, 30 mV_{rms}) to COM pin. Gradually raise frequency and measure frequency when read register D6 becomes 1.	
	ST_{CCH}	ST_{CCH} = Δf ÷ 15.734 kHz Δf: Difference between f and 15.734 kHz f: Input signal (17.0 kHz, 30 mV_{rms}) to COM pin. Gradually lower frequency and measure frequency when read register D6 becomes 1.	
SAP detection input sensitivity	SAP_{SENCE}	SAP_{SENCE} : Input signal level of COM pin (input signal: 78.67 kHz) When read register D5 changes from 0 to 1	SAP
SAP detection hysteresis	SAP_{HY}	SAP_{HY} =20 log (SAP_{SENCE} ÷ V) SAP_{SENCE}: SAP detection input sensitivity V: Input signal level of COM pin (Input signal: 78.67 kHz) When read register D5 is first set to 1, input signal level is gradually lowered until D5 becomes 0.	
Noise detection input sensitivity	NO_{SENCE}	NO_{SENCE}: Input signal level of COM pin Read register D4: Apply 6-V DC voltage to SDT pin to change it to 0 Read register D4: Input signal (160 kHz, 10 mV_{rms}) to COM pin. Raise the frequency until the DC voltage of the NDT pin reaches the maximum level, and then, while maintaining the frequency level, gradually raise the input signal level until D4 becomes 1.	SAP
Noise detection hysteresis	NO_{HY}	NO_{HY} = 20 log (NO_{SENCE} ÷ V) NO_{SENCE}: Noise detection input sensitivity V: Input signal level of NDT pin COM pin: Signal (160 kHz, 10 mV_{rms}) input After read register D4 is set to 1, raise the frequency until the DC voltage of the NDT pin reaches the maximum level, and then, while maintaining the frequency level, gradually lower the input signal level until D4 becomes 0.	
Monaural total output voltage	V_{OMO}	V_{OMO} : Output voltage of FOL and FOR pins COM pin: Monaural signal (300 Hz, 100 % modulation) input	Monaural
Stereo total output voltage	V_{OST}	L-channel V_{OST} : Output voltage of FOL pin COM pin: Stereo signal (L-only, 300 Hz, 100 % modulation) input R-channel V_{OST} : Output voltage of FOR pin COM pin: Stereo signal (R-only, 300 Hz, 100 % modulation) input	Stereo

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	User Mode Note
SAP total output voltage	V_{OSAP1}	V_{OSAP1} : Output voltage of FOL and FOR pins COM pin: SAP signal (300 Hz, 100 % modulation) input	SAP1
Difference between monaural L and R output voltage	V_{OLR}	V_{OLR} = 20 log (V_L ÷ V_R) V_L: Output voltage of FOL pin COM pin: Monaural signal (300 Hz, 100 % modulation) input V_R: Output voltage of FOR pin COM pin: Monaural signal (300 Hz, 100 % modulation) input	Monaural
Monaural total frequency characteristics 1	V_{OMO1}	V_{OMO1} = 20 log {V(1k) ÷ V(300)} V(1k): Output voltage of FOL pin COM pin: Monaural signal (1 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Monaural signal (300 Hz, 30 % modulation) input	Monaural
Monaural total frequency characteristics 2	V_{OMO2}	V_{OMO2} = 20 log {V(3k) ÷ V(300)} V(3k): Output voltage of FOL pin COM pin: Monaural signal (3 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Monaural signal (300 Hz, 30 % modulation) input	
Monaural total frequency characteristics 3	V_{OMO3}	V_{OMO3} = 20 log {V(8k) ÷ V(300)} V(8k): Output voltage of FOL pin COM pin: Monaural signal (8 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Monaural signal (300 Hz, 30 % modulation) input	
Monaural total frequency characteristics 4	V_{OMO4}	V_{OMO4} = 20 log {V(12k) ÷ V(300)} V(12k): Output voltage of FOL pin COM pin: Monaural signal (12 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Monaural signal (300 Hz, 30 % modulation) input	
Stereo total frequency characteristics 1	V_{OST1}	V_{OST1} = 20 log {V(1k) ÷ V(300)} V(1k): Output voltage of FOL pin COM pin: Stereo signal (L-only, 1 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Stereo signal (L-only, 300 Hz, 30 % modulation) input	Stereo
Stereo total frequency characteristics 2	V_{OST2}	V_{OST2} = 20 log {V(3k) ÷ V(300)} V(3k): Output voltage of FOL pin COM pin: Stereo signal (L-only, 3 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Stereo signal (L-only, 300 Hz, 30 % modulation) input	
Stereo total frequency characteristics 3	V_{OST3}	V_{OST3} = 20 log {V(8k) ÷ V(300)} V(8k): Output voltage of FOL pin COM pin: Stereo signal (L-only, 8 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Stereo signal (L-only, 300 Hz, 30 % modulation) input	
Stereo total frequency characteristics 4	V_{OST4}	V_{OST4} = 20 log {V(12k) ÷ V(300)} V(12k): Output voltage of FOL pin COM pin: Stereo signal (L-only, 12 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: Stereo signal (L-only, 300 Hz, 30 % modulation) input	

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	User Mode Note
SAP total frequency characteristics 1	V_{OSAP11}	V_{OSAP11} = 20 log {V(1k) ÷ V(300)} V(1k): Output voltage of FOL pin COM pin: SAP signal (1 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: SAP signal (300 Hz, 30 % modulation) input	SAP1
SAP total frequency characteristics 2	V_{OSAP12}	V_{OSAP12} = 20 log {V(3k) ÷ V(300)} V(3k): Output voltage of FOL pin COM pin: SAP signal (3 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: SAP signal (300 Hz, 30 % modulation) input	
SAP total frequency characteristics 3	V_{OSAP13}	V_{OSAP13} = 20 log {V(8k) ÷ V(300)} V(8k): Output voltage of FOL pin COM pin: SAP signal (8 kHz, 30 % modulation) input V(300): Output voltage of FOL pin COM pin: SAP signal (300 Hz, 30 % modulation) input	
Stereo channel separation 1	Sep_1	L-channel Sep_1 = 20 log (V_L ÷ V_R) V_L: Output voltage of FOL pin COM pin: Stereo signal (L-only, 300 Hz, 30% modulation) input V_R: Output voltage of FOR pin COM pin: Stereo signal (L-only, 300 Hz, 30 % modulation) input R-channel Sep_1 = 20 log (V_R ÷ V_L) V_R: Output voltage of FOR pin COM pin: Stereo signal (R-only, 300 Hz, 30 % modulation) input V_L: Output voltage of FOL pin COM pin: Stereo signal (R-only, 300 Hz, 30 % modulation) input	Stereo
Stereo channel separation 2	Sep_2	L-channel Sep_2 = 20 log (V_L ÷ V_R) V_L: Output voltage of FOL pin COM pin: Stereo signal (L-only, 1 kHz, 30 % modulation) input V_R: Output voltage of FOR pin COM pin: Stereo signal (L-only, 1 kHz, 30 % modulation) input R-channel Sep_2 = 20 log (V_R ÷ V_L) V_R: Output voltage of FOR pin COM pin: Stereo signal (R-only, 1 kHz, 30 % modulation) input V_L: Output voltage of FOL pin COM pin: Stereo signal (R-only, 1 kHz, 30 % modulation) input	
Stereo channel separation 3	Sep_3	L-channel Sep_3 = 20 log (V_L ÷ V_R) V_L: Output voltage of FOL pin COM pin: Stereo signal (L-only, 3 kHz, 30 % modulation) input V_R: Output voltage of FOR pin COM pin: Stereo signal (L-only, 3 kHz, 30 % modulation) input R-channel Sep_3 = 20 log (V_R ÷ V_L) V_R: Output voltage of FOR pin COM pin: Stereo signal (R-only, 3 kHz, 30 % modulation) input V_L: Output voltage of FOL pin COM pin: Stereo signal (R-only, 3 kHz, 30 % modulation) input	

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	User Mode Note
Stereo channel separation 4	Sep_4	L-channel $Sep_4 = 20 \log (V_L \div V_R)$ V_L: Output voltage of FOL pin COM pin: Stereo signal (L-only, 5 kHz, 30 % modulation) input V_R: Output voltage of FOR pin COM pin: Stereo signal (L-only, 5 kHz, 30 % modulation) input R-channel $Sep_4 = 20 \log (V_R \div V_L)$ V_R: Output voltage of FOR pin COM pin: Stereo signal (R-only, 5 kHz, 30 % modulation) input V_L: Output voltage of FOL pin COM pin: Stereo signal (R-only, 5 kHz, 30 % modulation) input	Stereo
Stereo channel separation 5	Sep_5	L-channel $Sep_5 = 20 \log (V_L \div V_R)$ V_L: Output voltage of FOL pin COM pin: Stereo signal (L-only, 8 kHz, 30 % modulation) input V_R: Output voltage of FOR pin COM pin: Stereo signal (L-only, 8 kHz, 30 % modulation) input R-channel $Sep_5 = 20 \log (V_R \div V_L)$ V_R: Output voltage of FOR pin COM pin: Stereo signal (R-only, 8 kHz, 30 % modulation) input V_L: Output voltage of FOL pin COM pin: Stereo signal (R-only, 8 kHz, 30 % modulation) input	
Monaural total harmonic distortion	THD_{MO}	THD_{MO} : Distortion rate of FOL and FOR pins COM pin: Monaural signal (1 kHz, 100 % modulation) input	Monaural
Stereo total harmonic distortion 1	THD_{ST1}	L-channel THD_{ST1} : Distortion rate of FOL pin COM pin: Stereo signal (L-only, 1 kHz, 100 % modulation) input R-channel THD_{ST1} : Distortion rate of FOR pin COM pin: Stereo signal (R-only, 1 kHz, 100 % modulation) input	Stereo
Stereo total harmonic distortion 2	THD_{ST2}	L-channel THD_{ST2} : Distortion rate of FOL pin COM pin: Stereo signal (L-only, 8 kHz, 30 % modulation) input R-channel THD_{ST2} : Distortion rate of FOR pin COM pin: Stereo signal (R-only, 8 kHz, 30 % modulation) input	
SAP total harmonic distortion	THD_{SAP}	THD_{SAP} : Distortion rate of FOL and FOR pins COM pin: SAP signal (1 kHz, 100 % modulation) input	SAP1
Crosstalk 1 (SAP→Stereo)	CT_1	$CT_1 = 20 \log (V_{CT1} \div 500 \text{ mV})$ V_{CT1}: Measure output voltage of FOL or FOR pins after BPF (1 kHz) SAP: 1 kHz, 100 % modulation Stereo: Pilot signal only, 0 % modulation	Stereo
Crosstalk 2 (Stereo→SAP)	CT_2	$CT_2 = 20 \log (V_{CT2} \div 500 \text{ mV})$ V_{CT2}: Measure output voltage of FOL or FOR pins after BPF (1 kHz) Stereo: 1 kHz, 100 % modulation SAP: Carrier only, 0 % modulation	SAP1

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	User Mode Note
Monaural total S/N	S/N_{MO}	L-channel S/N_{MO} = 20 log (V_{OMOL} ÷ V_L) V_{OMOL} : Output voltage of FOL pin after LPF (30 kHz) COM pin: Monaural signal (300 Hz, 100 % modulation) input V_L: Output voltage of FOL pin (no signal) R-channel S/N_{MO} = 20 log (V_{OMOR} ÷ V_R) V_{OMOR}: Output voltage of FOR pin after LPF (30 kHz) COM pin: Monaural signal (300 Hz, 100 % modulation) input V_R: Output voltage of FOR pin (no signal)	Monaural
Stereo total S/N	S/N_{ST}	L-channel S/N_{ST} = 20 log (V_{OSTL} ÷ V_L) V_{OSTL} : Output voltage of FOL pin after LPF (30 kHz) COM pin: Stereo signal (L-only, 300 Hz, 100 % modulation) input V_L: Output voltage of FOL pin COM pin: Pilot signal input R-channel S/N_{ST} = 20 log (V_{OSTR} ÷ V_R) V_{OSTR} : Output voltage of FOR pin after LPF (30 kHz) COM pin: Stereo signal (R-only, 300 Hz, 100 % modulation) input V_R: Output voltage of FOR pin COM pin: Pilot signal input	Stereo
SAP total S/N	S/N_{SAP}	L-channel S/N_{SAP} = 20 log (V_{OSAP1L} ÷ V_L) V_{OSAP1L} : Output voltage of FOL pin after LPF (30 kHz) COM pin: SAP signal (300 Hz, 100 % modulation) input V_L: Output voltage of FOL pin COM pin: SAP carrier (0 % modulation) input R-channel S/N_{SAP} = 20 log (V_{OSAP1R} ÷ V_R) V_{OSAP1R} : Output voltage of FOR pin after LPF (30 kHz) COM pin: SAP signal (300 Hz, 100 % modulation) input V_R: Output voltage of FOR pin COM pin: SAP carrier (0 % modulation) input	SAP1
Total muting level	Mute	Mute = 20 log (V_{OMOL} ÷ V_M) V_{OMOL} : Output voltage of LOT pin COM pin: Monaural signal (1 kHz, 100 % modulation) input V_M : Output voltage of LOT pin Write register 06H, D0: 0 COM pin: Monaural signal (1 kHz, 100 % modulation) input	Monaural mute
Timing current	I_T	I_T : Current that flows from V_{CC} to STI, WTI pins STI, WTI pins : 6 V DC is applied.	
Inter-mode DC offset 1	V_{DOF1}	V_{DOF1} = V_{MONO} – V_{Mute} V_{MONO} : DC voltage at LOT and ROT pins User mode : Monaural NDT pin: 6 V DC is applied. V_{Mute} : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1: 0) NDT pin: 6 V DC is applied.	Mute to Monaural

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	User Mode Note
Inter-mode DC offset 2	V_{DOF2}	$V_{DOF2} = V_{ST} - V_{Mute}$ V_{ST} : DC voltage at LOT and ROT pins User mode : Stereo NDT pin: 6 V DC is applied. V_{Mute} : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1: 0) NDT pin: 6 V DC is applied.	Mute to Stereo
Inter-mode DC offset 3	V_{DOF3}	$V_{DOF3} = V_{SAP} - V_{Mute}$ V_{SAP} : DC voltage at LOT and ROT pins User mode : SAP1 NDT pin: 6 V DC is applied. V_{Mute} : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1: 0) NDT pin: 6 V DC is applied.	Mute to SAP1
Inter-mode DC offset 4	V_{DOF4}	$V_{DOF4} = V_{MONO} - V_{Mute}$ V_{MONO} : DC voltage at LOT and ROT pins User mode : External input NDT pin: 6 V DC is applied. V_{Mute} : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1: 0) NDT pin: 6 V DC is applied.	Mute to External input
Surround output characteristics 1	V_{SR1L}	$V_{SR1L} = 20 \log (V_{L1} \div V_{EL})$ V_{L1}: Output voltage of LOT pin V_{EL}: Input voltage of EL1, EL2 pins (100 Hz, 150 mV_{rms}) ER1, ER2 pins: No signal Surround: ON (Subaddress 04H, Bit D6: 1)	External input 1 External input 2
Surround output characteristics 2	V_{SR2L}	V_{SR2L} : $20 \log (V_{L2} \div V_{EL})$ V_{L2}: Output voltage of LOT pin V_{EL}: Input voltage of EL1, EL2 pins (1 kHz, 150 mV_{rms}) ER1, ER2 pins: No signal Surround: ON (Subaddress 04H, Bit D6: 1)	
Surround output characteristics 3	V_{SR3L}	V_{SR3L} : $20 \log (V_{L3} \div V_{EL})$ V_{L3}: Output voltage of LOT pin V_{EL}: Input voltage of EL1, EL2 pins (10 kHz, 150 mV_{rms}) ER1, ER2 pins: No signal Surround: ON (Subaddress 04H, Bit D6: 1)	
Surround output characteristics 4	V_{SR4R}	V_{SR4R} : $20 \log (V_{R} \div V_{EL})$ V_{R}: Output voltage of ROT pin V_{EL}: Input voltage of EL1, EL2 pins (1 kHz, 150 mV_{rms}) ER1, ER2 pins: No signal Surround: ON (Subaddress 04H, Bit D6: 1)	

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	Sub-address	Data	User Mode Note
Low frequency band width boost control	V_{BB}	Bass response = 20 log (V_{OUT} ÷ V_{IN}) V_{IN}: Input signal level (sine wave: 100 Hz, 150 mV_{rms}) of external input 1 (EL1, ER1 pins) or external input 2 (EL2, ER2 pins) V_{OUT}: Output signal level of LOT, ROT pins	09H	3FH	External input 1, External input 2
Low frequency band width cut control	V_{BC}			00H	
High frequency band width boost control	V_{TB}	Treble response = 20 log (V_{OUT} ÷ V_{IN}) V_{IN}: Input signal level (sine wave: 10 kHz, 150 mV_{rms}) of external input 1 (EL1, ER1 pins) or external input 2 (EL2, ER2 pins) V_{OUT}: Output signal level of LOT, ROT pins	0AH	3FH	
High frequency band width cut control	V_{TC}			00H	
Volume attenuation 1	ATT_{VL1}	Volume attenuation = 20 log (V_{OUT} ÷ V_{IN}) V_{IN}: Input signal level (sine wave: 1 kHz, 500 mV_{rms}) of external input 1 (EL1, ER1 pins) or external input 2 (EL2, ER2 pins) V_{OUT}: Output signal level of LOT, ROT pins	07H	3FH	External input 1, External input 2
Volume attenuation 2	ATT_{VL2}			20H	
Volume attenuation 3	ATT_{VL3}			00H	
Balance attenuation L-ch 1	ATT_{BL1}	Balance attenuation = 20 log (V_{OUT} ÷ V_{IN}) V_{IN}: Input signal level (sine wave: 1 kHz, 500 mV_{rms}) of external input 1 (EL1 pin) or external input 2 (EL2 pin) V_{OUT}: Output signal level of LOT pin	08H	3FH	External input 1, External input 2
Balance attenuation L-ch 2	ATT_{BL2}			30H	
Balance attenuation L-ch 3	ATT_{BL3}			20H	
Balance attenuation L-ch 4	ATT_{BL4}			00H	
Balance attenuation R-ch 1	ATT_{BR1}	Balance attenuation = 20 log (V_{OUT} ÷ V_{IN}) V_{IN}: Input signal level (sine wave: 1 kHz, 500 mV_{rms}) of external input 1 (ER1 pin) or external input 2 (ER2 pin) V_{OUT}: Output signal level of ROT pin	08H	3FH	External input 1, External input 2
Balance attenuation R-ch 2	ATT_{BR2}			20H	
Balance attenuation R-ch 3	ATT_{BR3}			10H	
Balance attenuation R-ch 4	ATT_{BR4}			00H	
Difference between monaural L and R output voltage 1 (in case of external input)	V_{OLR1}	Error between channels = 20 log (V_{ROUT} ÷ V_{RIN}) – 20 log (V_{LOUT} ÷ V_{LIN}) External input 1 V_{ROUT}: Output signal level of ROT pin V_{RIN}: Input signal level of ER1 pin (sine wave: 1 kHz, 500 mV_{rms}) V_{LOUT}: Output signal level of LOT pin V_{LIN}: Input signal level of EL1 pin (sine wave: 1 kHz, 500 mV_{rms}) External input 2 V_{ROUT}: Output signal level of ROT pin V_{RIN}: Input signal level of ER2 pin (sine wave: 1 kHz, 500 mV_{rms}) V_{LOUT}: Output signal level of LOT pin V_{LIN}: Input signal level of EL2 pin (sine wave: 1 kHz, 500 mV_{rms})	07H	3FH	External input 1, External input 2
Difference between monaural L and R output voltage 2 (in case of external input)	V_{OLR2}			20H	
Difference between monaural L and R output voltage 3 (in case of external input)	V_{OLR3}			10H	

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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Parameter	Symbol	Test Conditions	Sub-address	Data	User Mode [Note]
Crosstalk 3 TV signal → External input	CT_3	$CT_3 = 20 \log (V_{EXT} \div V_{TV})$ V_{EXT}: Output voltage of LOT or ROT pin when the input select 1 is set to the external input 1 or 2 (the data of bits D6 and D5 of subaddress 06H are "01" or "10"). V_{TV}: Output voltage ROT or LOT pin when the input select 1 is set to the TV signal (the data of bits D6 and D5 of subaddress 06H are "00"). COM pin: Monaural, stereo or SAP signal (1 kHz, 100 % modulation) input External input 1 (EL1, ER1 pins), external input 2 (EL2, ER2 pins): No input Measure the values of the external inputs 1 and 2 individually.	07H	3FH	External input 1, External input 2, Stereo, SAP, Monaural
Crosstalk 4 L-ch → R-ch	CT_4	$CT_4 = 20 \log (V_{EXTR} \div V_{EXTL})$ V_{EXTR}: Output voltage of ROT pin when the input select 1 is set to the external input 1 or 2 (the data of bits D6 and D5 of subaddress 06H are "01" or "10"). V_{EXTL}: Output voltage LOT pin when the input select 1 is set to the external input 1 or 2 (the data of bits D6 and D5 of subaddress 06H are "01" or "10"). EL1, EL2 pins: External input signal (1 kHz, 500 mV_{rms}) input ER1, ER2 pins: No input Measure the values of the external inputs 1 and 2 individually.	07H	3FH	External input 1, External input 2
Total harmonic distortion (in case of external input)	THD_{EXT}	THD_{EXT}: Total harmonic distortion rate of LOT, ROT pins External input 1 (EL1, ER1 pins), external input 2 (EL2, ER2 pins): External input signal (1 kHz, 500 mV_{rms}) input	07H	3FH	External input 1, External input 2
Maximum input voltage of external input	V_{IEM}	V_{IEM}: Maximum input voltage level External input 1 (EL1, ER1 pins), external input 2 (EL2, ER2 pins): External input signal (1 kHz) input when the total harmonic distortion rate of LOT and ROT pins becomes 1 %.	07H	3FH	External input 1, External input 2
Output noise (in case of external input)	NO	NO: Output noise of LOT, ROT pins through DIN/AUDIO External input 1 (EL1, ER1 pins), external input 2 (EL2, ER2 pins): No input (grounded through the resistor (R_g = 600 Ω))	07H	3FH	External input 1, External input 2

Note For details about the User Mode, refer to **5. MODE MATRIX**.

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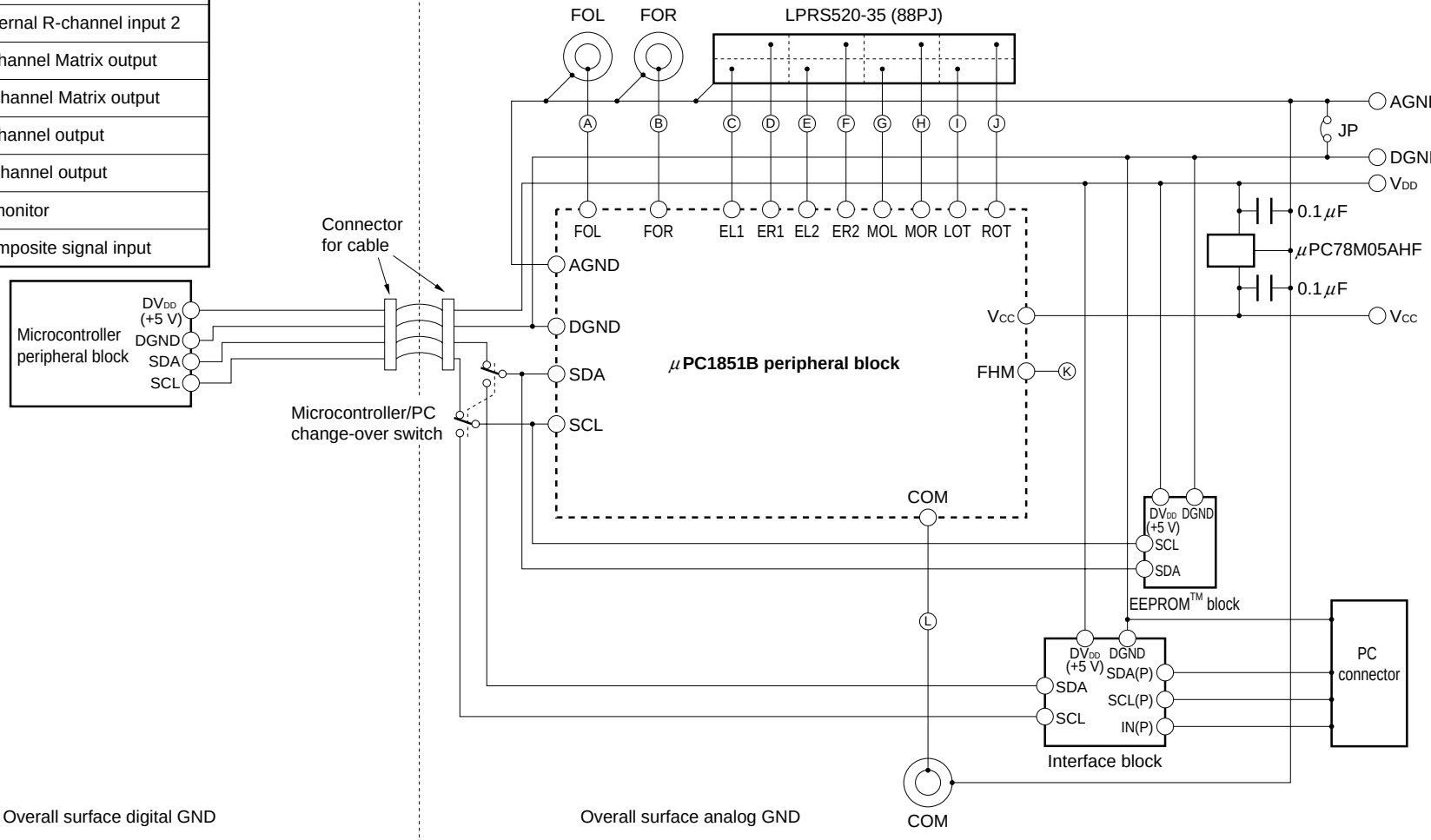
9. TEST CIRCUIT

Test Points

A	L-channel fixed output
B	R-channel fixed output
C	External L-channel input 1
D	External R-channel input 1
E	External L-channel input 2
F	External R-channel input 2
G	L-channel Matrix output
H	R-channel Matrix output
I	L-channel output
J	R-channel output
K	f_H monitor
L	Composite signal input



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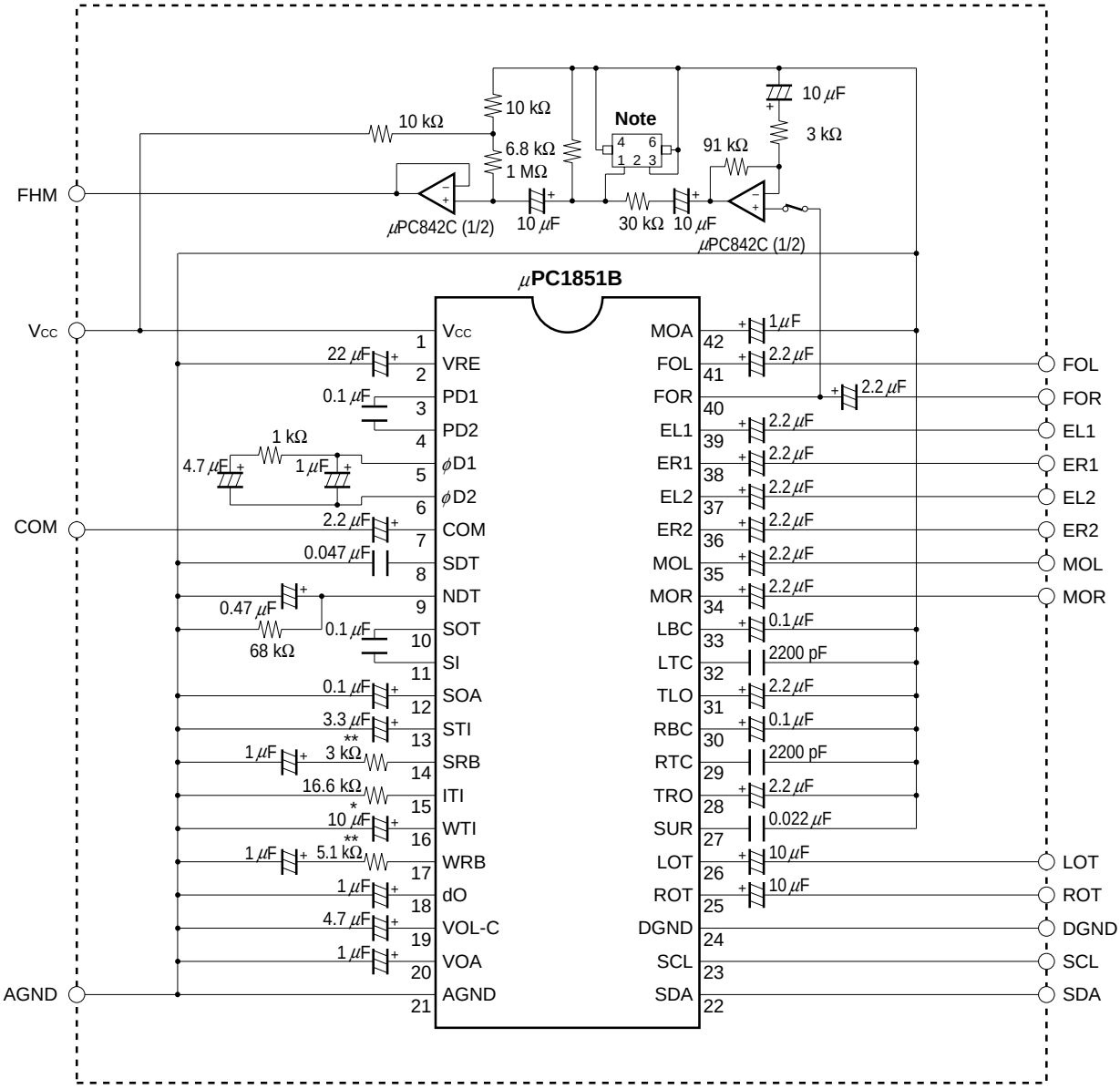
μPC1851B Peripheral Block



Note Filter: 126XGS-7990Z, TOKO

Remark Use the followings for external parts.

Resistor (*): Metal film resistor (±1 %). Unless otherwise specified; ±5 %

Capacitors (**): Tantalum capacitor (±10 %). Unless otherwise specified, ±20 %

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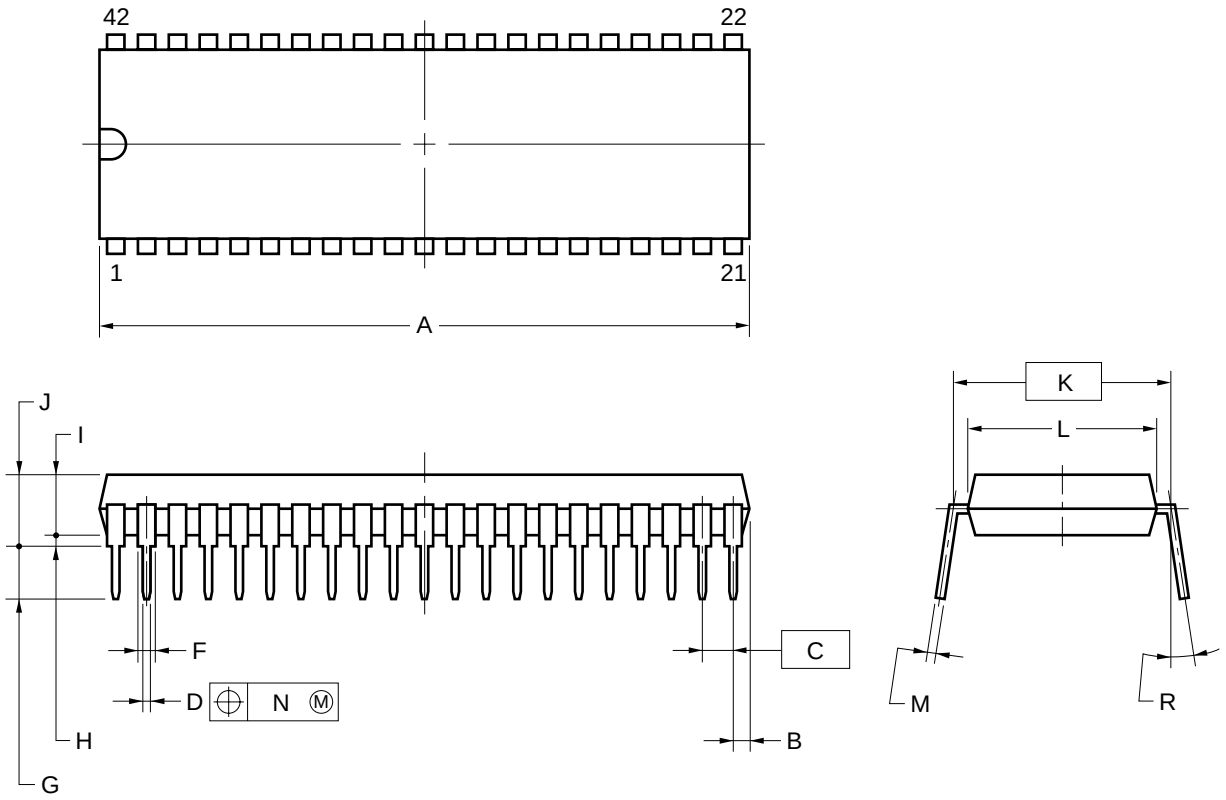
10. PACKAGE DRAWINGS

42-PIN PLASTIC SDIP (15.24mm(600))



NOTES

1. Each lead centerline is located within 0.17 mm of its true position (T.P.) at maximum material condition.

2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	39.13 MAX.
B	1.78 MAX.
C	1.778 (T.P.)
D	0.50±0.10
F	0.85 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.17
R	0~15°

P42C-70-600B-2

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11. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

μPC1851BCU: 42-pin plastic SDIP (15.24 mm (600))

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead)

Caution The wave soldering process must be applied only to leads, and the make sure that the package body does not get jet soldered.

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